

MODEL NAME : *Echo 15 17 nVidia*

PCB NO : *LA-B751P/LA-B753P*

BOM P/N : *4319UA31L01 / 4319UA31L02 for NV*
4319UB31L01 for AMD

Compal Confidential

Echo 15 17 with nVidia GFX

Schematic Document

Broadwell H-type

Rev: 0.1(X00)

2014/01/02

@ : Nopop Component

EMC@ : EMI part

ESD@ : ESD part

RF@ : RF part

CONN@ : Connector Component

BDW@ : Intel BOARDWELL

AOAC@ : Intel AOAC

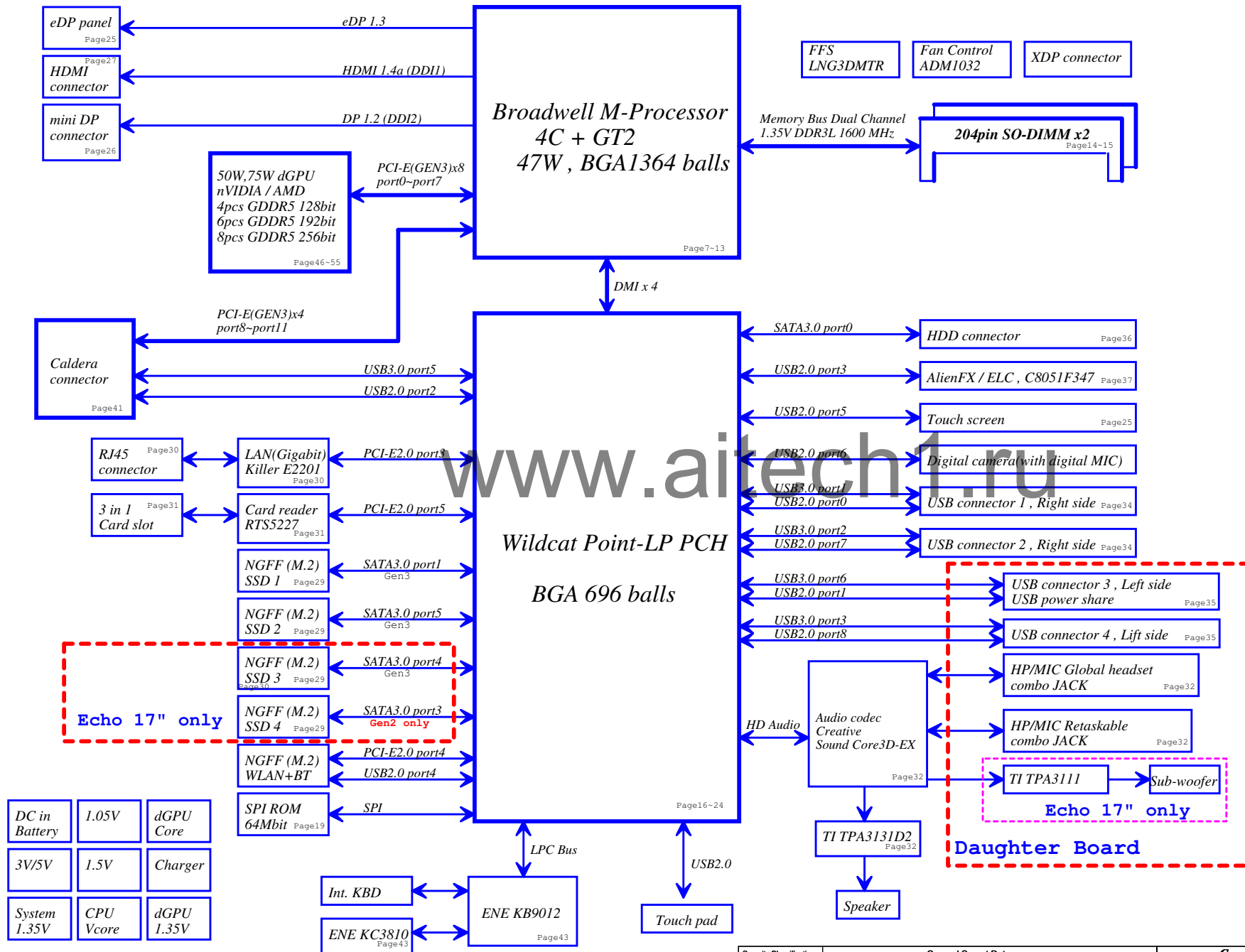
DIS@ : Discrete Part

NV@ AMD@ : Board ID

ZZZ1 PCB
DAB0000P000
PCB 18F LA-B752P REV0 M/B 8
12L

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				Date	Wednesday, March 26, 2014
				Sheet	1 of 69
				Rev	0.1

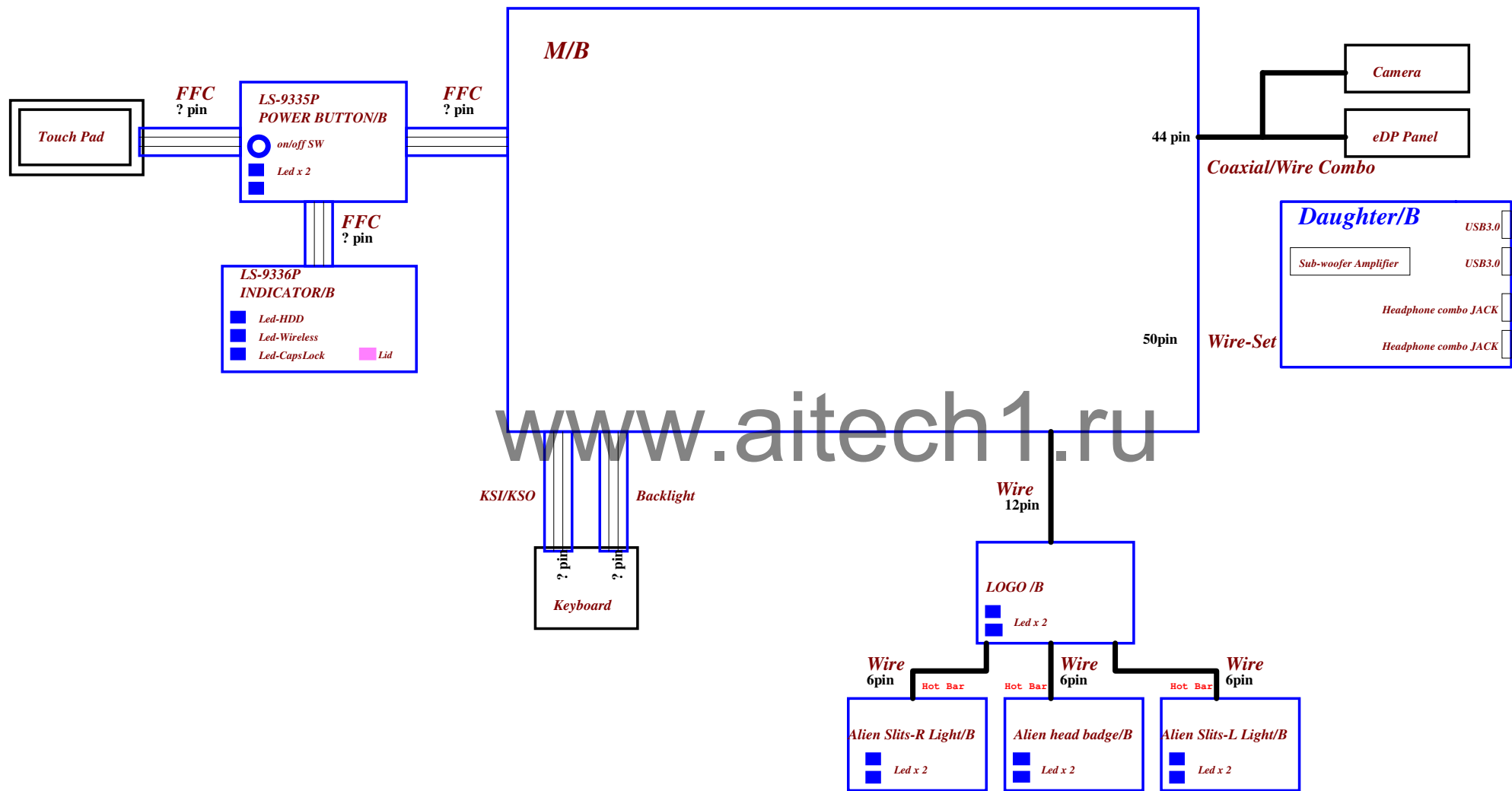
Echo 15"/17" Block Diagram



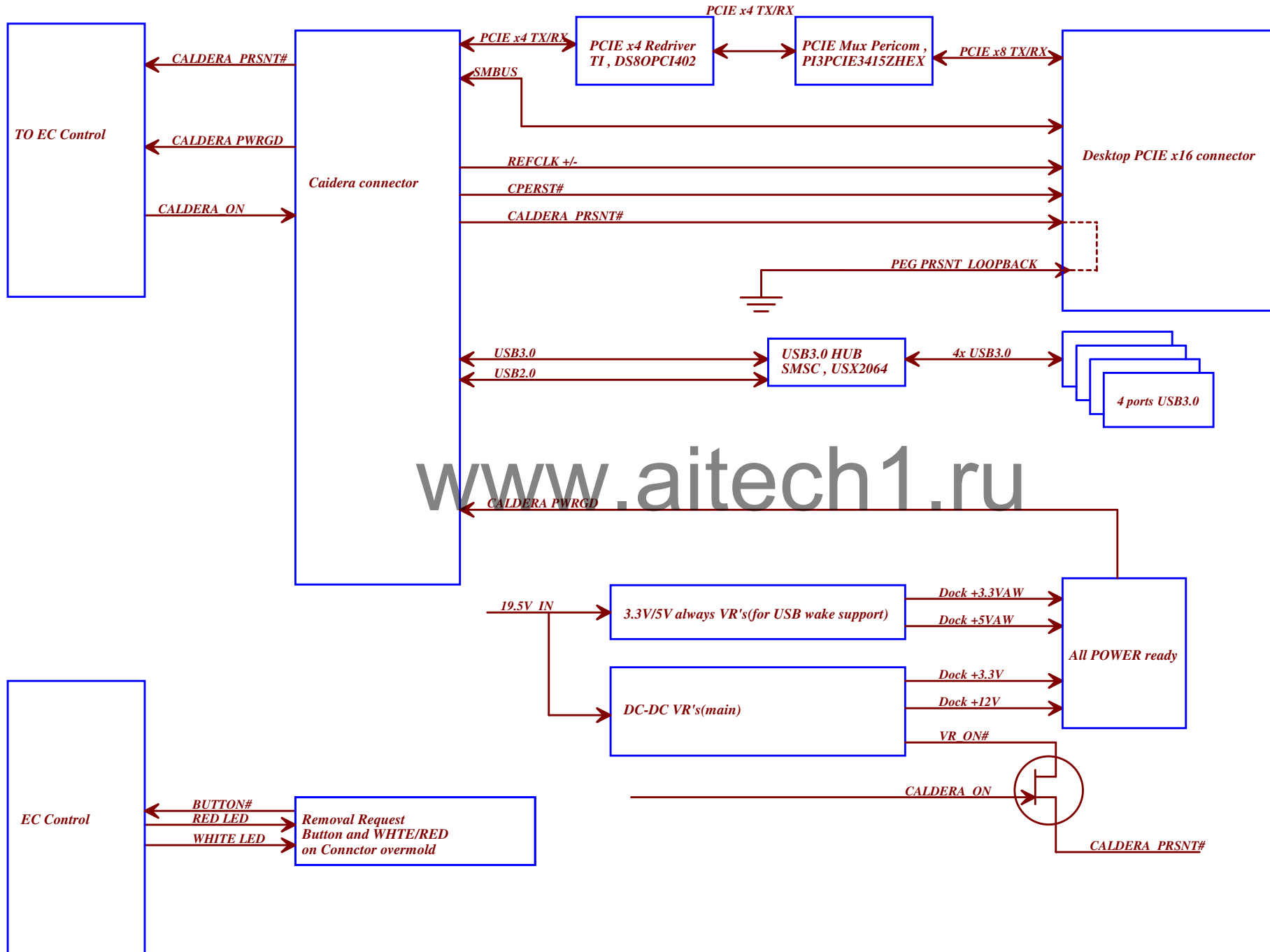
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Project Code : AAP10/AAP20

File Name : LA-XXXXP



Caldera(Echo graphic expander) block diagram



Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	NVIDIA Graphic
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	AMD Graphic
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE	
19	NC	3.000V	3.300V	3.300V	0xEE - 0xFF	

Board ID TABLE

ID		PCB Revision
NV	AMD	
0	10	EVT-1
1	11	DVT-1
2	12	DVT-2
3	13	MP

Symbol Note :

 : means Digital Ground

 : means Analog Ground

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CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N15P)
CLKOUT_PCIE5	DGPU (Caldera)

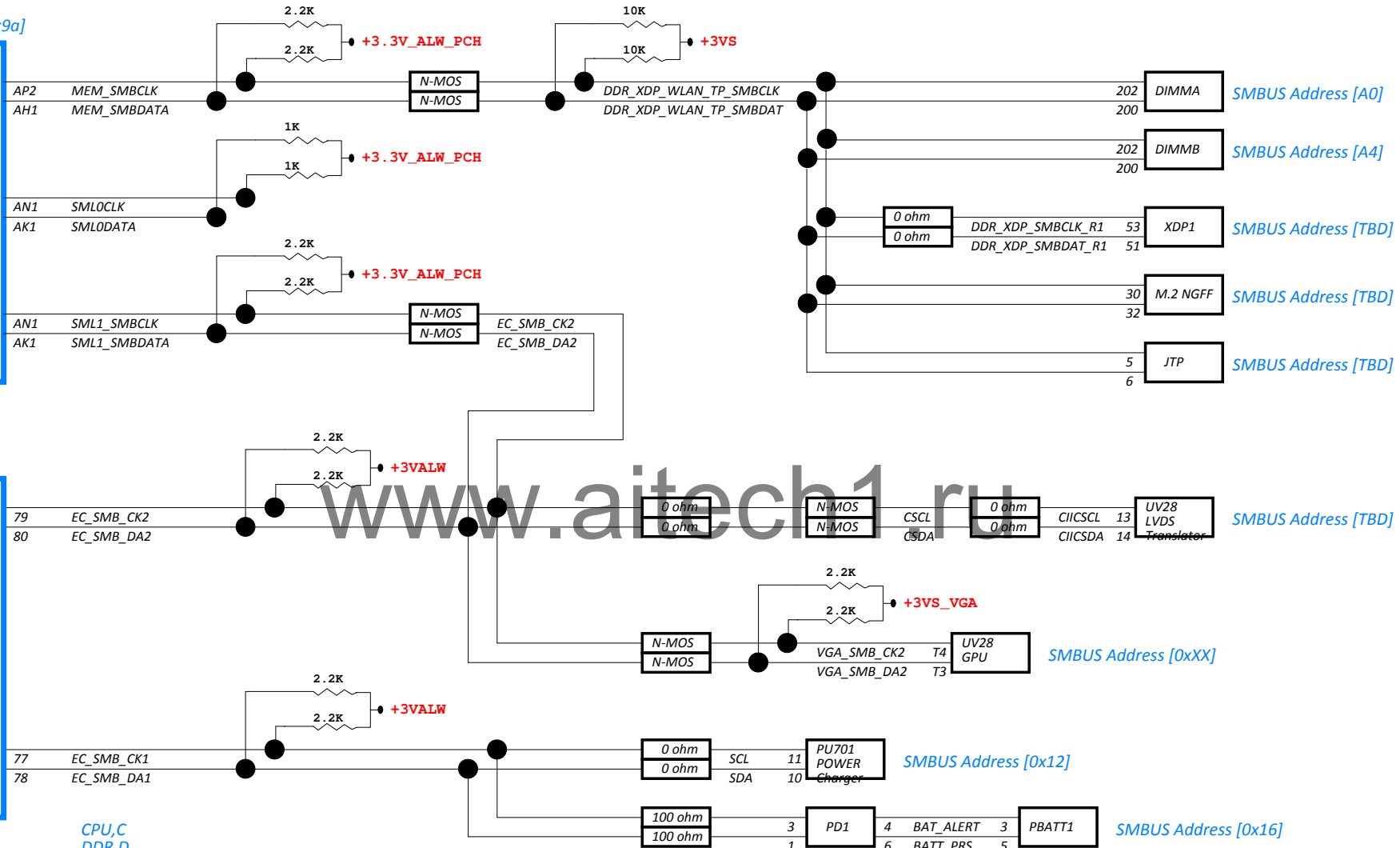
USB3.0	
Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2
USB2.0	
Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	
SATA	
SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

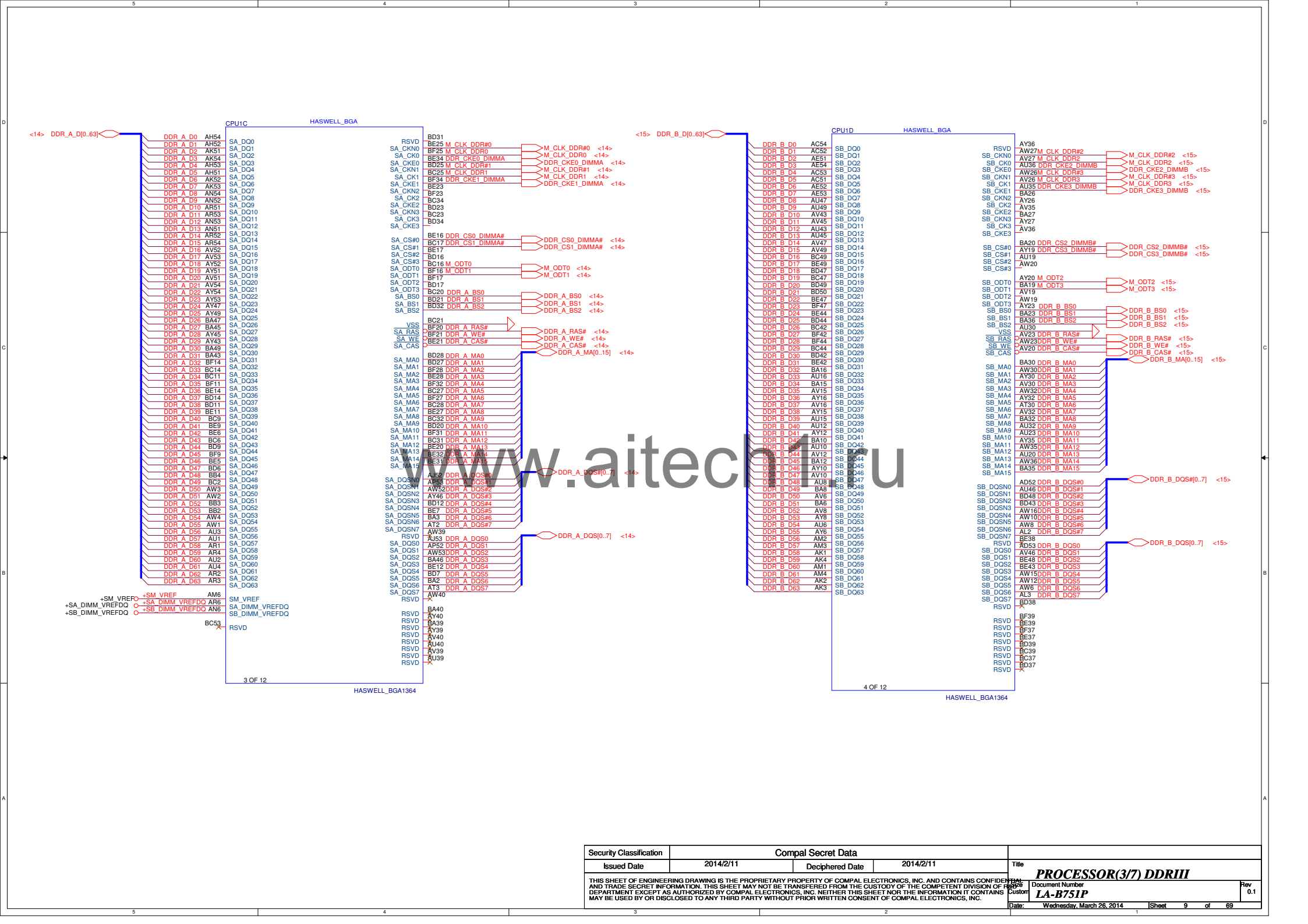
SMBUS Address [0x9a]

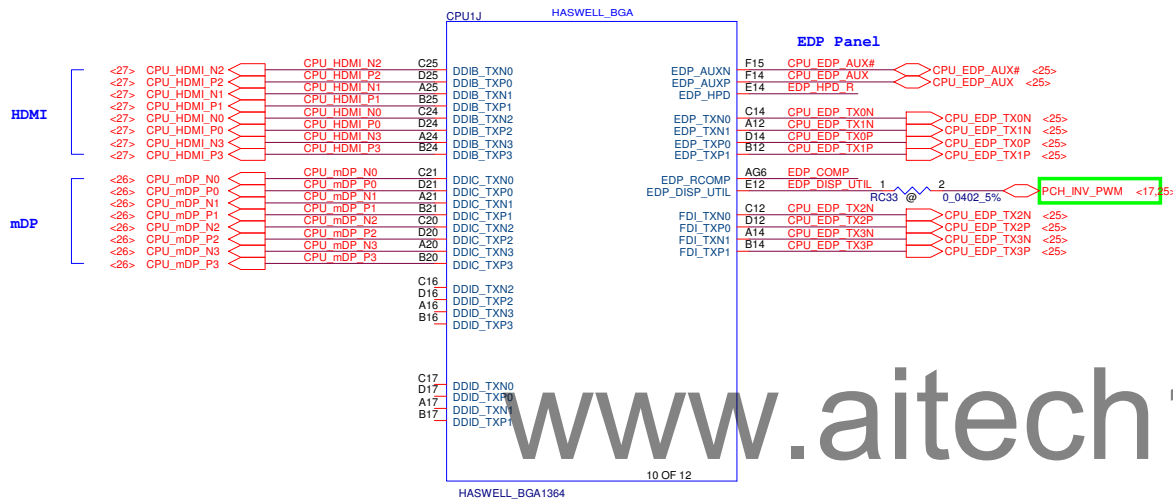
Broadwell

KBC
KB9012A4

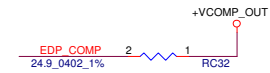
CPU,C
DDR,D
GPU,DP,HDMI,EDP,V
LAN,L
AUDIO,A
NGFF,N
USB,U
CALDERA,M
HDD,S
ELC,E
FAN,F
TP,T
KBC,K
DC,O





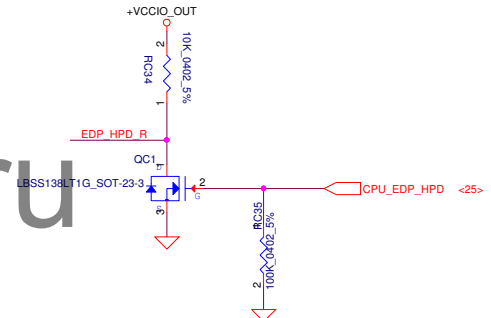


COMPENSATION PU FOR eDP



Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP

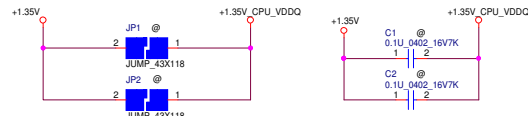


HPD is a active-high signal from device.
The HPD processor input is active-low signal.

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Date: Wednesday, March 26, 2014				Sheet	10 of 69

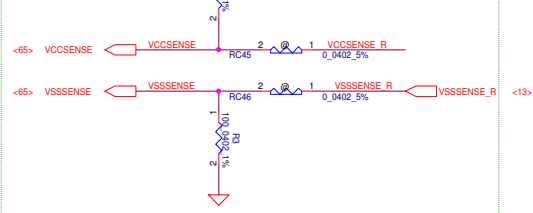
+1.35V_CPU_VDDQ Source

Note:
Intel Shark Bay
Removed the S3 power reduction circuit.



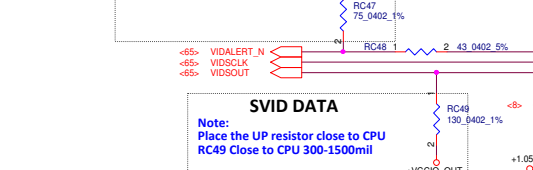
VCC_SENSE

Note:
0 ohm Resistor should be placed
close to CPU



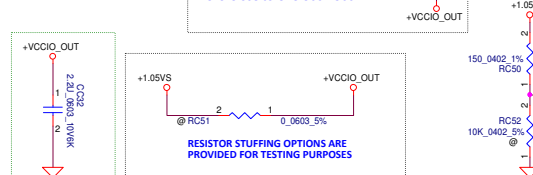
SVID ALERT

Note:
Place the UP resistor close to CPU
RC47 Close to CPU 300-1500mil

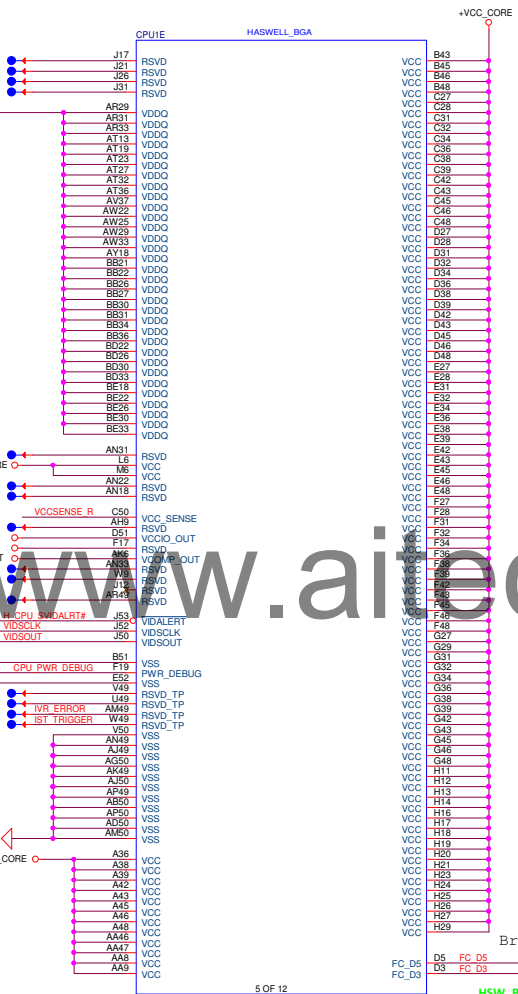
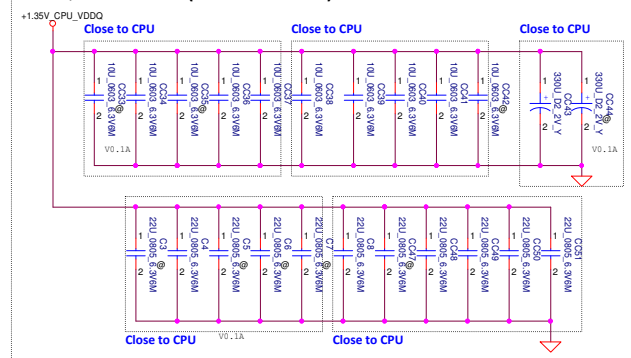


SVID DATA

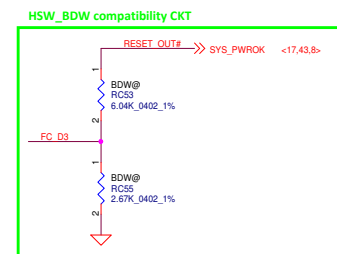
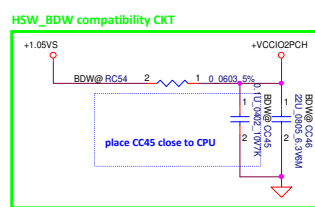
Note:
Place the UP resistor close to CPU
RC49 Close to CPU 300-1500mil

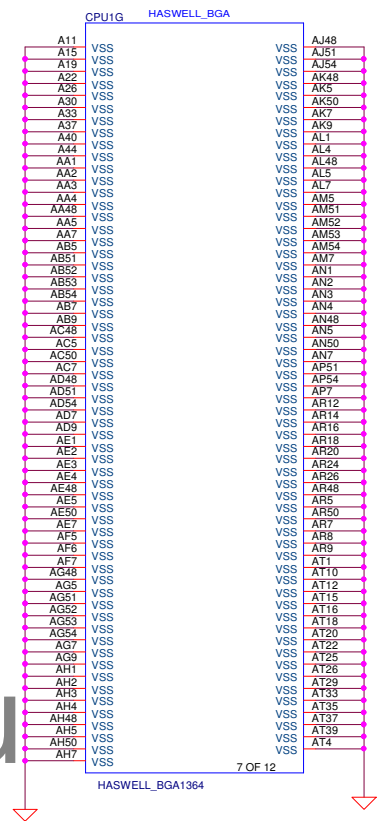


VDDQ DECOUPLING (Follow INTEL DG)

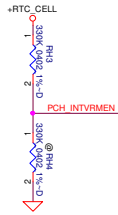


	HSW	BDW
RC54	X	V
CC45	X	V
CC46	X	V
RC53	X	V
RC55	X	V

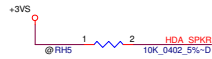




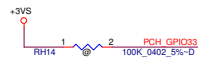
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				Document Number	0.1
Customer				LA-B751P Date: Wednesday, March 26, 2014 Sheet 13 of 69	



INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

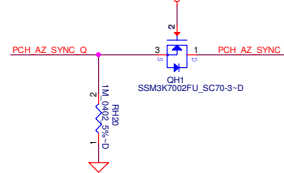


FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED

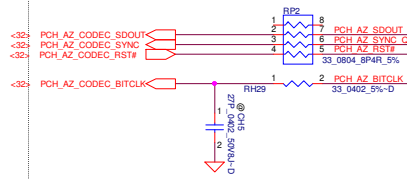
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

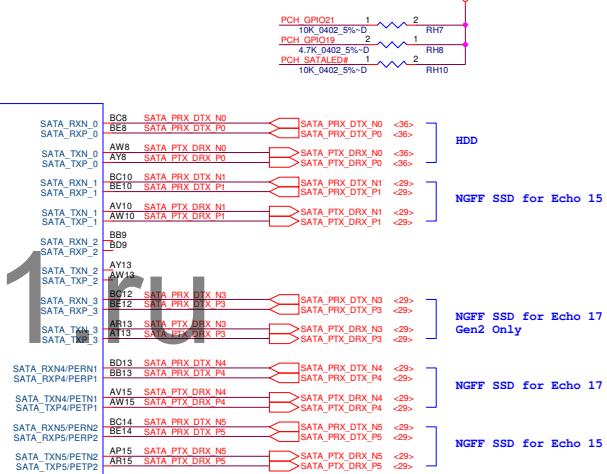
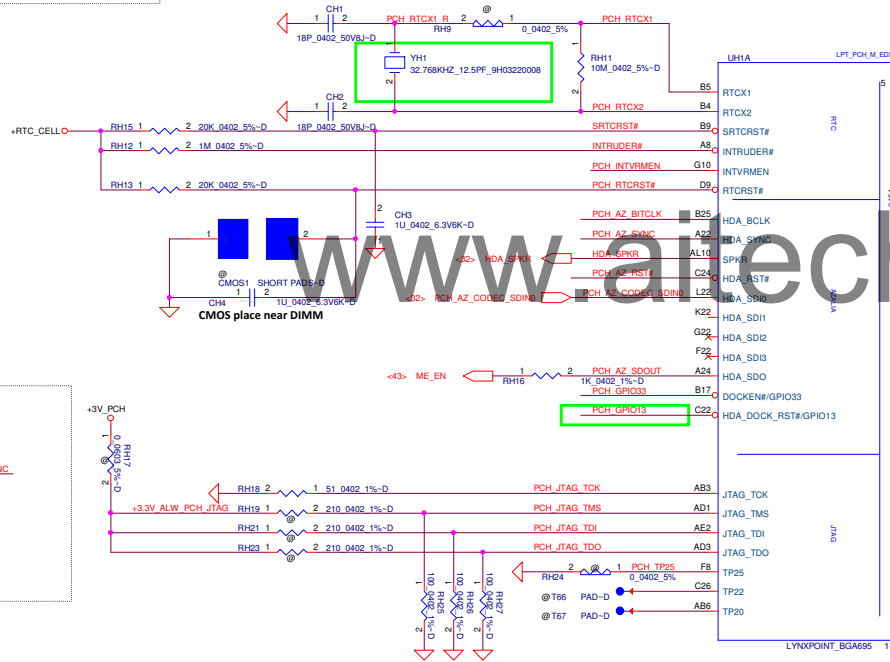
HDA_SYNC Isolation Circuit



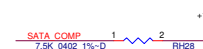
HDA for Codec and MDC



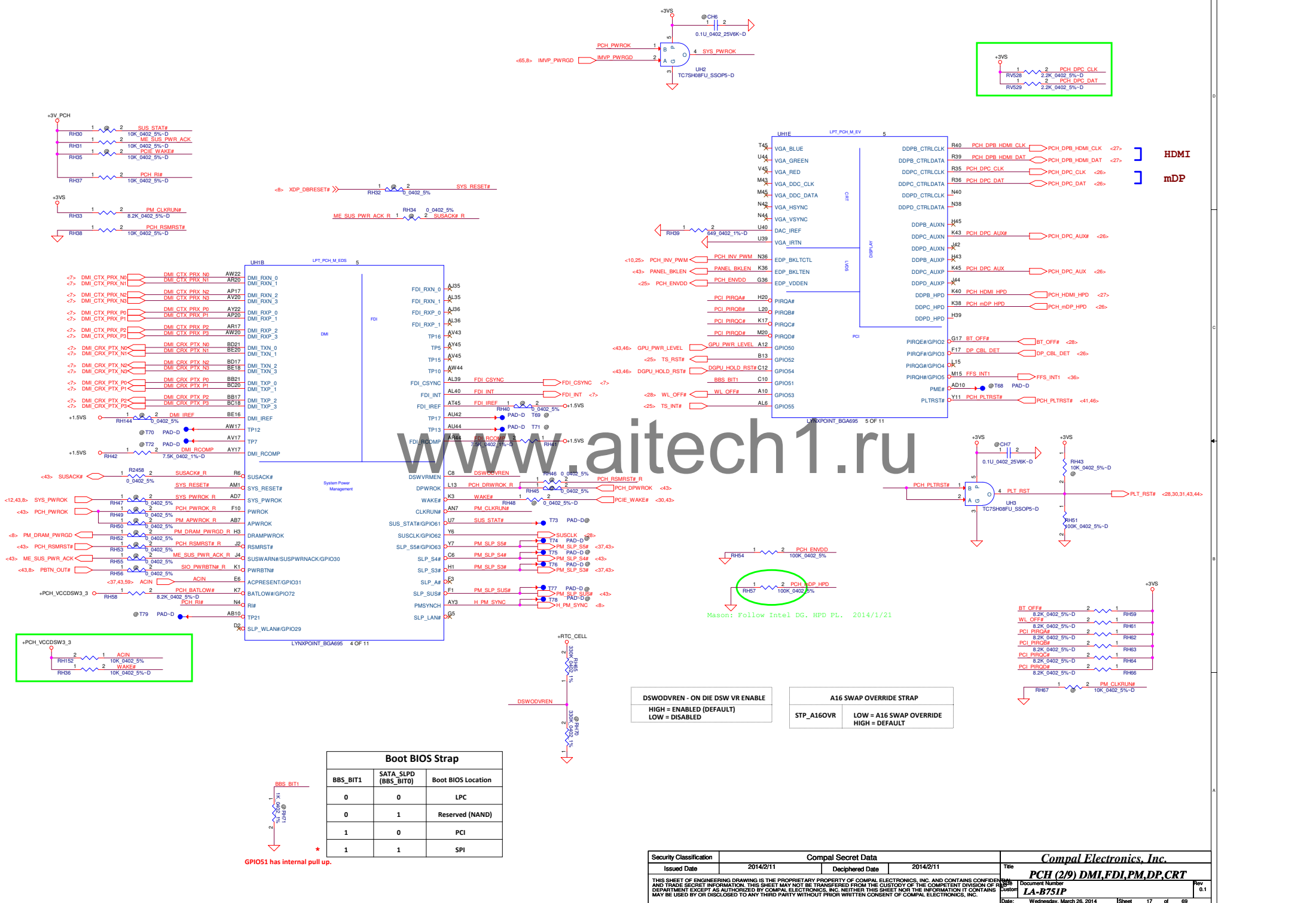
YH1 Change to SJ1000LD00 (ESR=50Kohm)



SATA Impedance Compensation



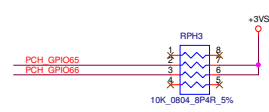
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.



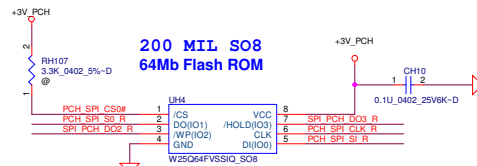
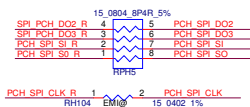
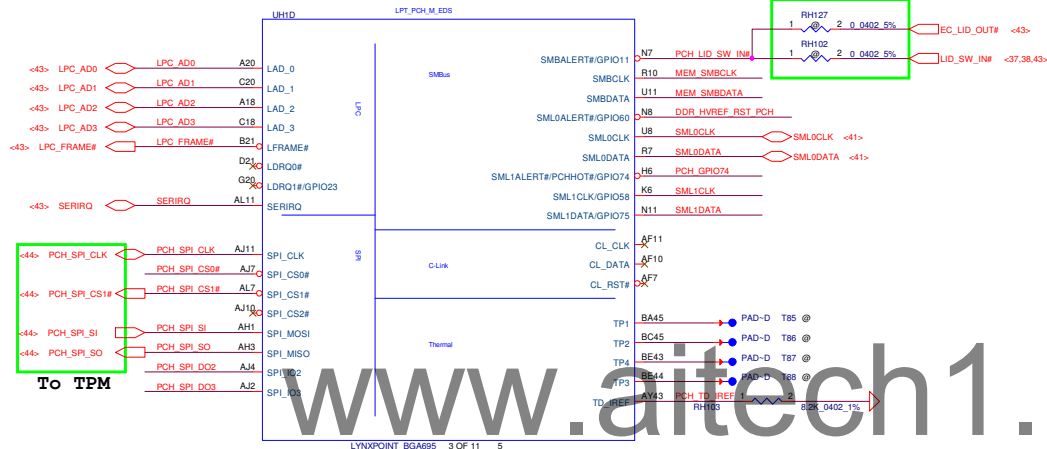
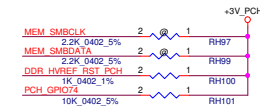
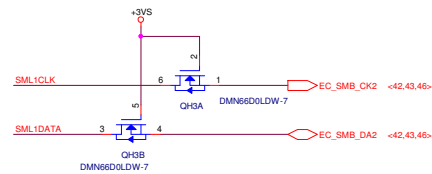
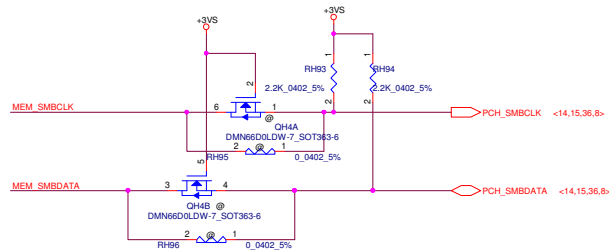
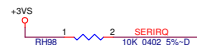
Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

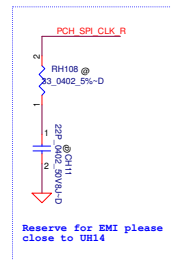
A16 SWAP OVERRIDE STRAP
STP_A160VR LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT



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			Date Wednesday, March 26, 2014	Sheet 18 of 69

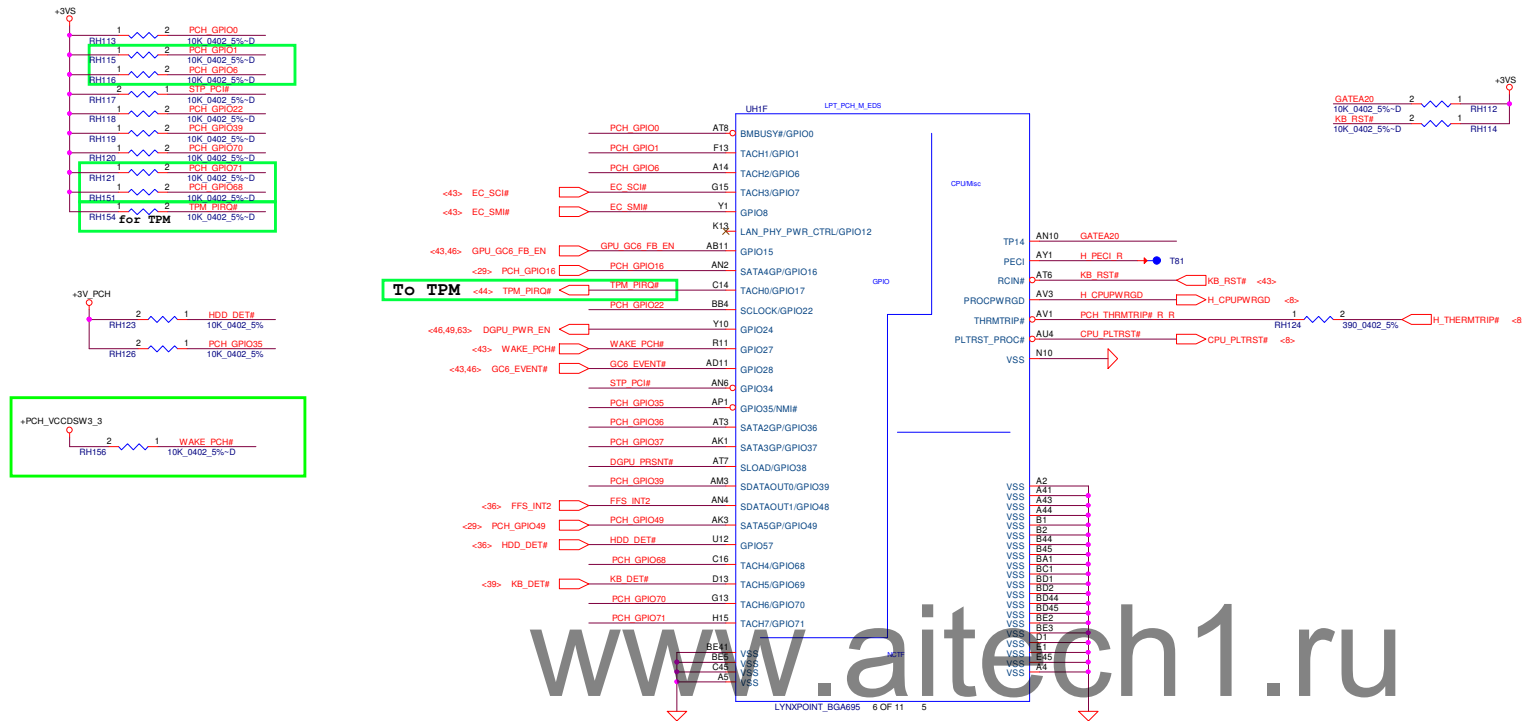


UH14 to SA000039A30 IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
 UH14 to SA000046400 IC FL 64M EN25Q64-104HIP SOIC 8P SPI ROM
 UH14 to SA00006N100 IC FL 64M MX25L647EM2I-10G SOIC 8P SPI ROM
 UH14 to SA00005L100 IC FL 64M N25Q064A13ESECOP SOIC 8P SPI ROM

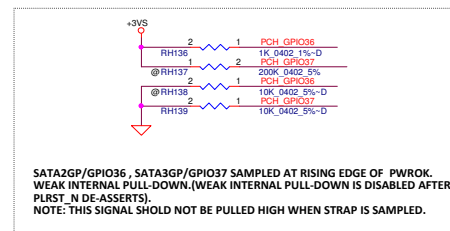
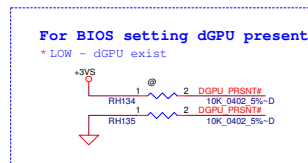




SD302100280 Chnage SD309100280 2/25 採購建議

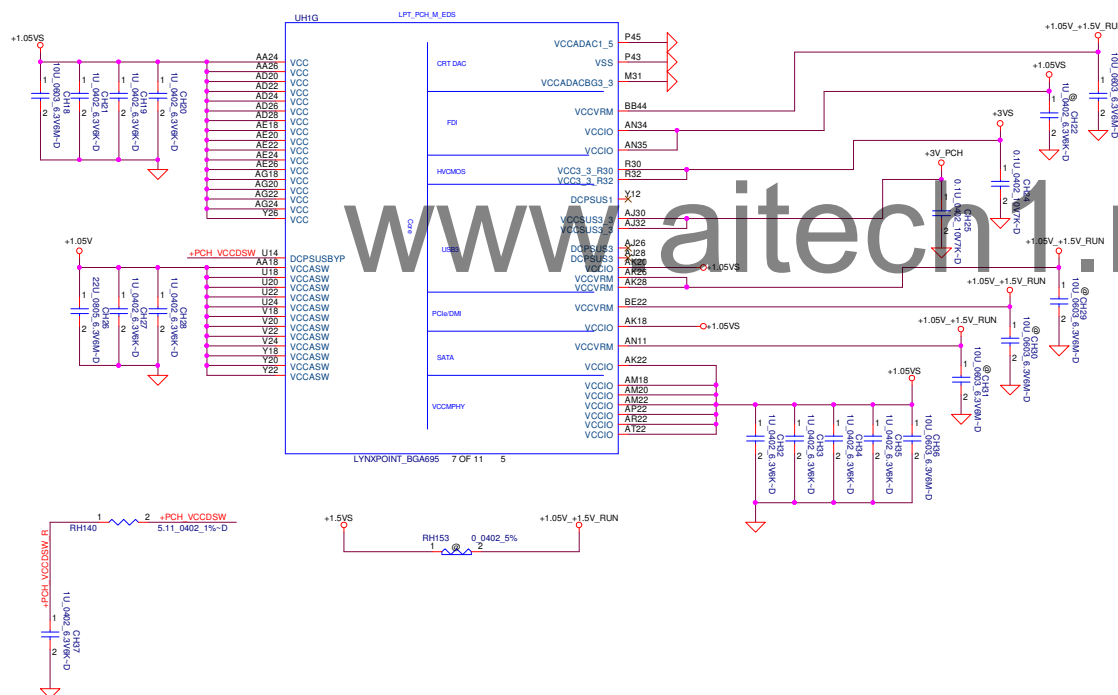


Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

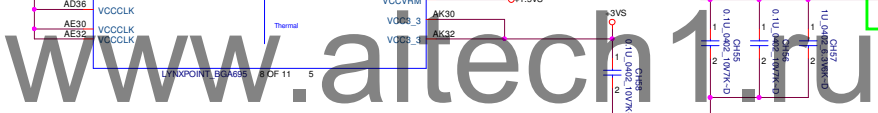


Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

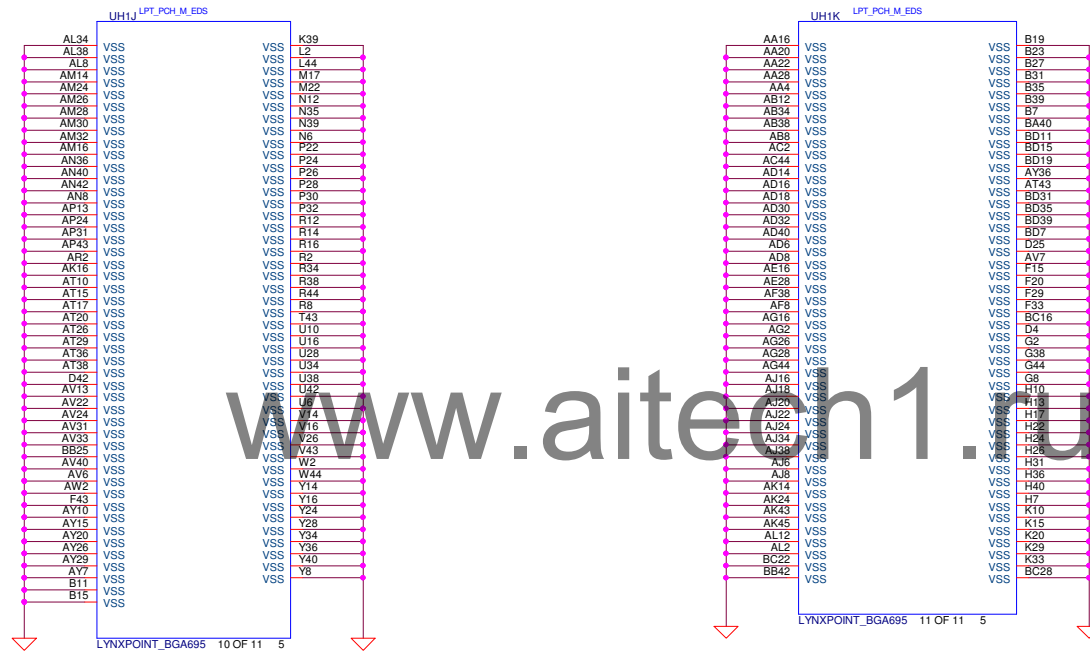
Same with 534345_PCH_LPT_9



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUS3_3	3.3V	0.01 A
VCCSUS3_3_3	3.3V	0.022 A
VCCDSW3_3	3.3V	0.261 A
V_PROC_IO	1.05V	0.004 A

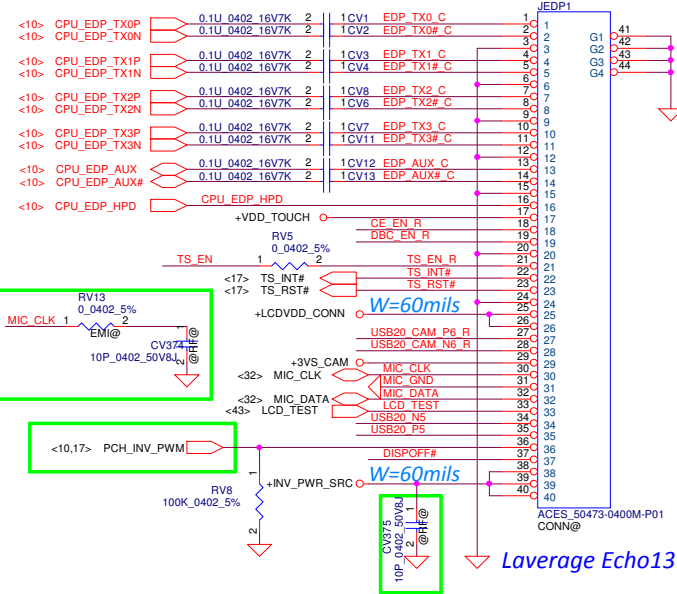
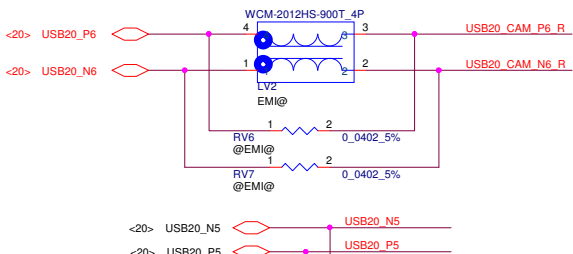
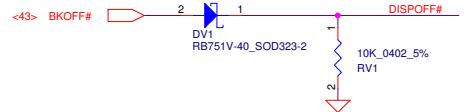
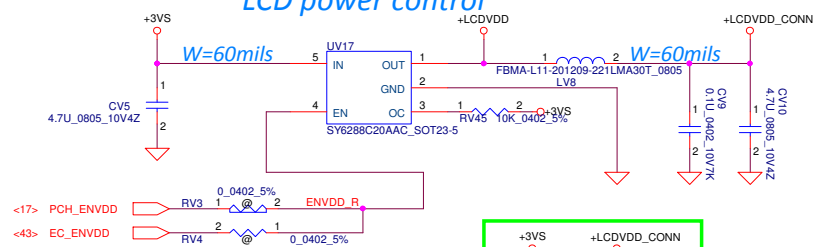


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				Doc Number	
				Date:	Wednesday, March 26, 2014
				Sheet	23 of 69

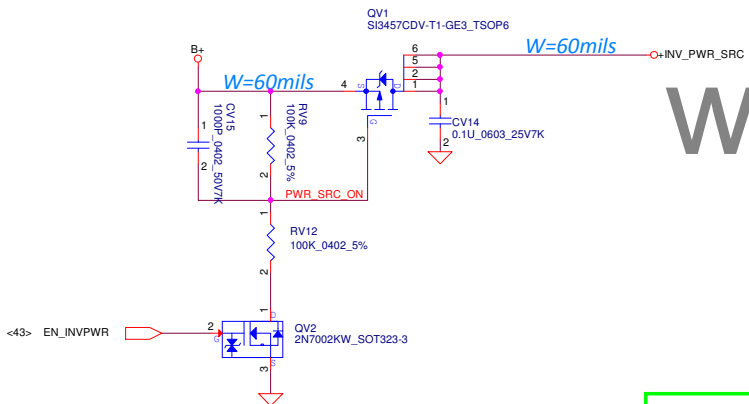


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				LA-B751P	0.1
				Date: Wednesday, March 26, 2014	Sheet 24 of 69

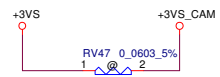
LCD power control



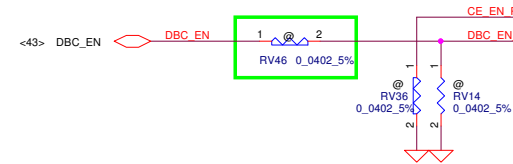
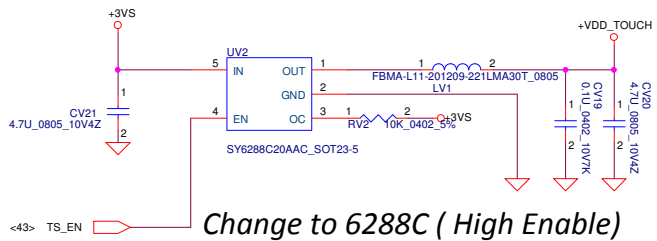
LCD backlight power control



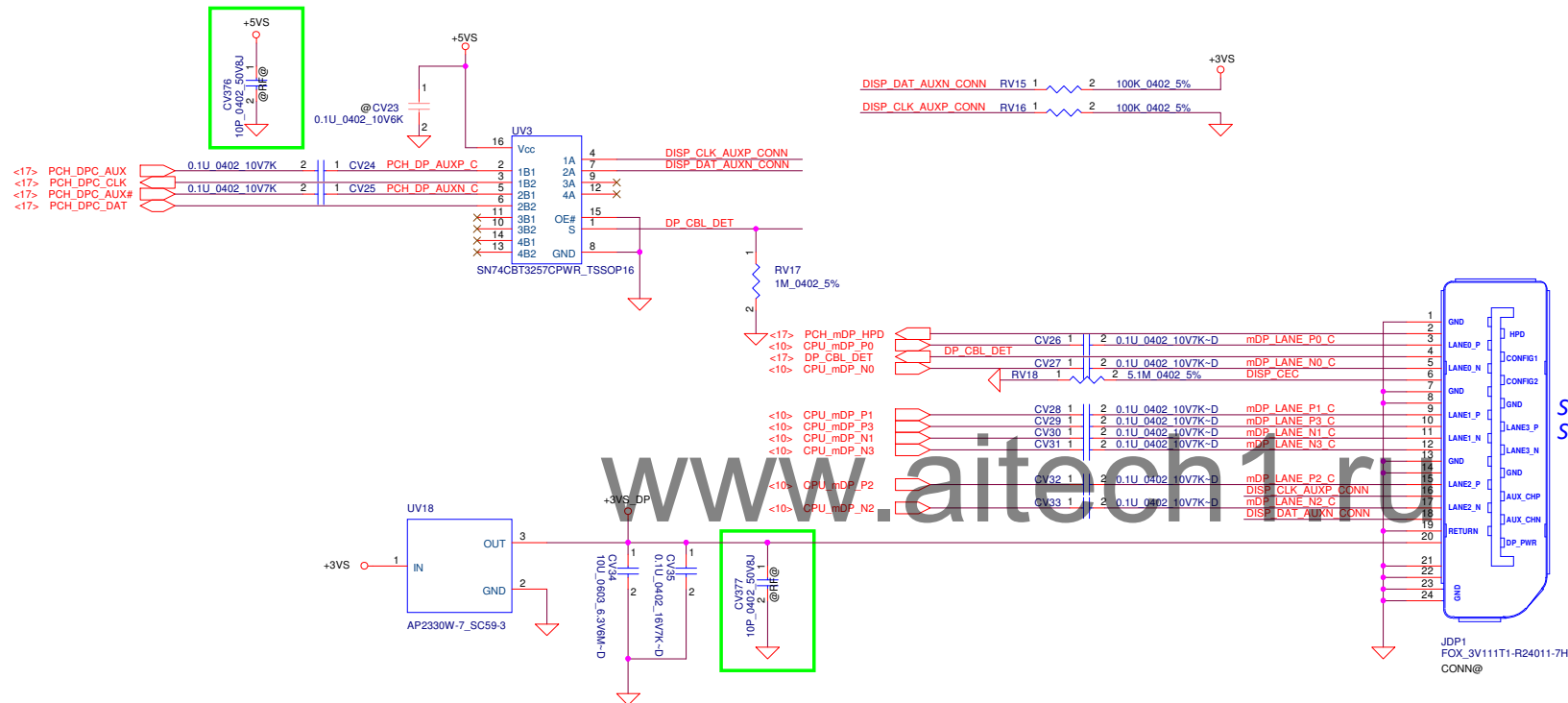
Webcam power control



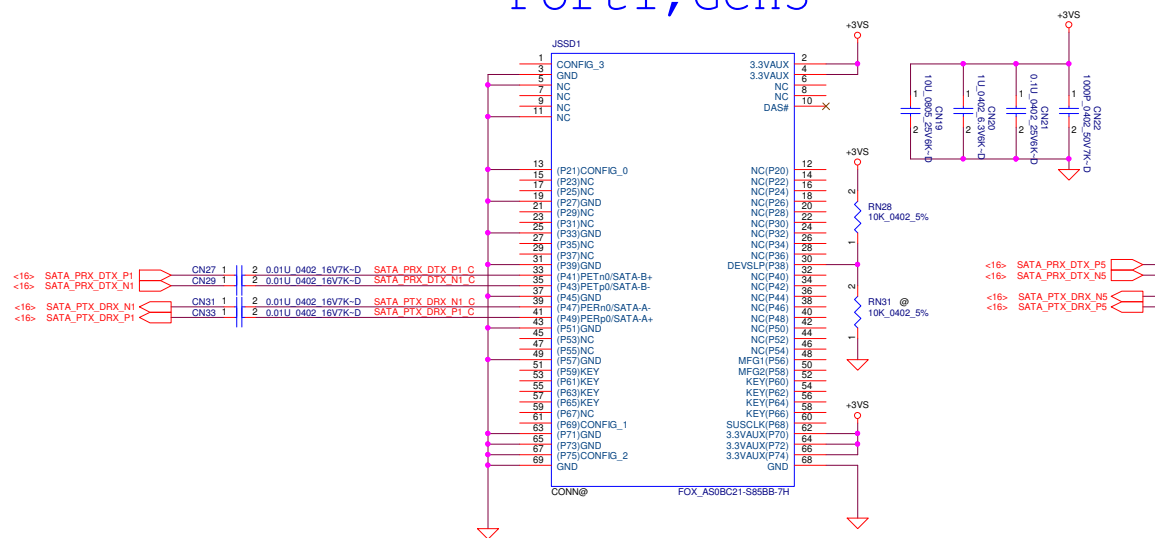
Touch screen panel power control



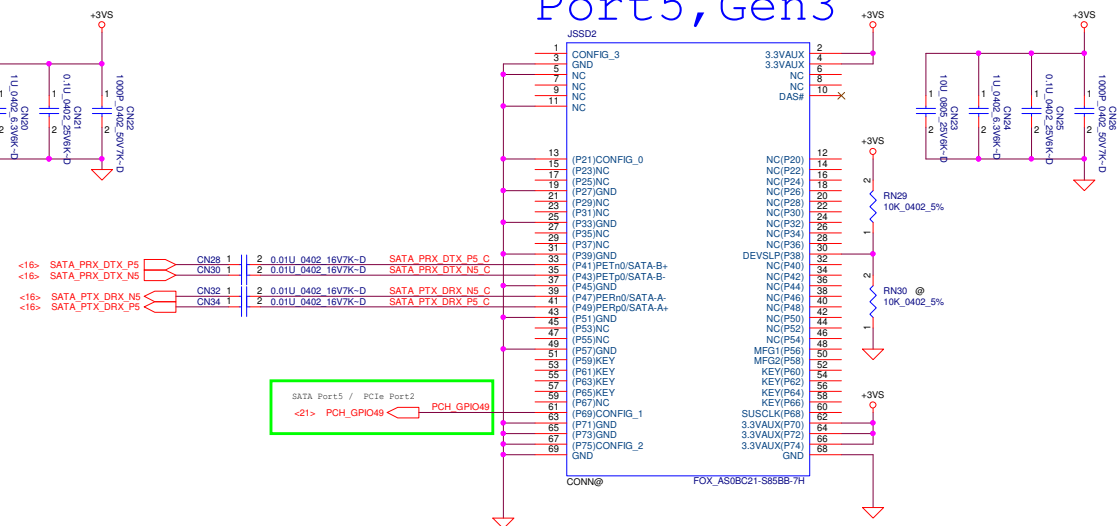
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	LCD Conn/Cam, Touch	
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				Date:	Wednesday, March 26, 2014	Sheet 25 of 69



Port1, Gen3

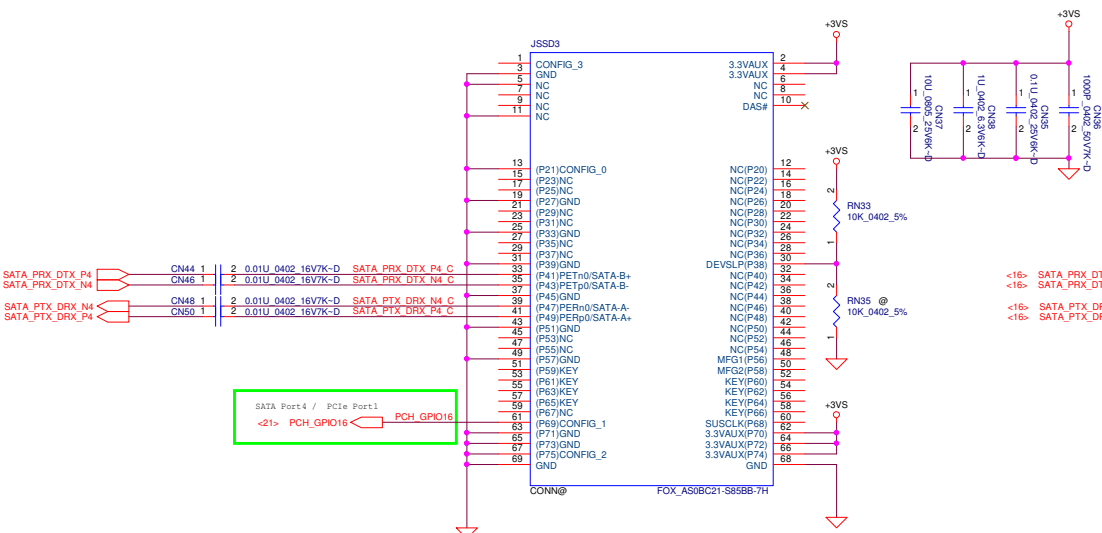


Port5, Gen3

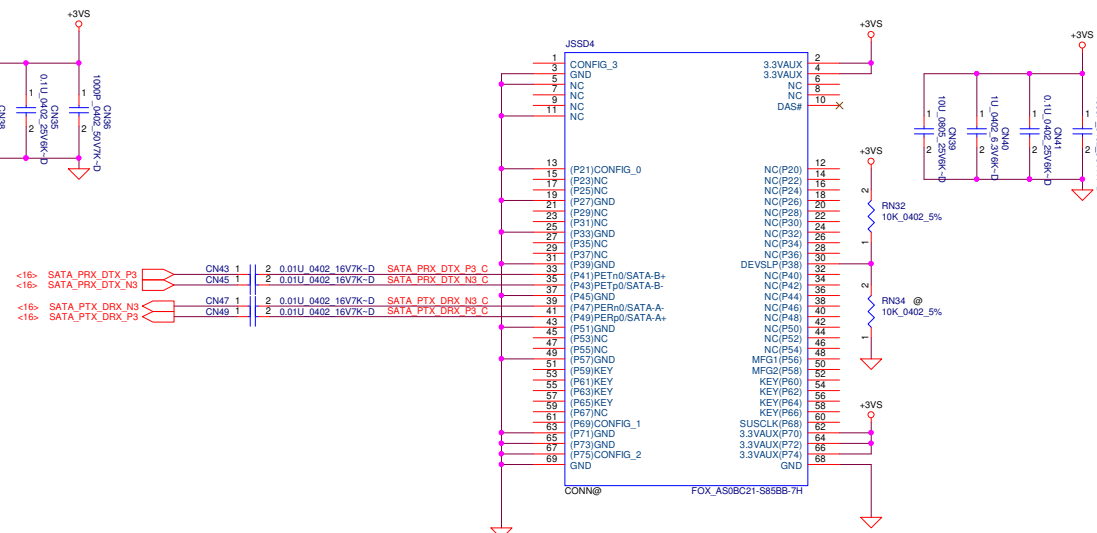


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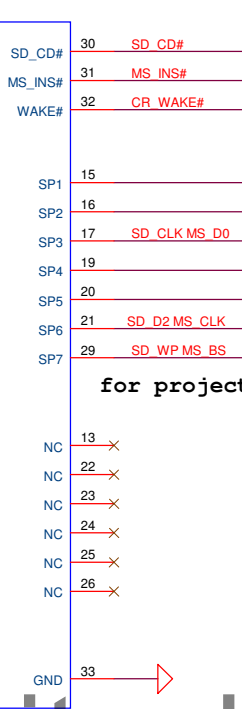
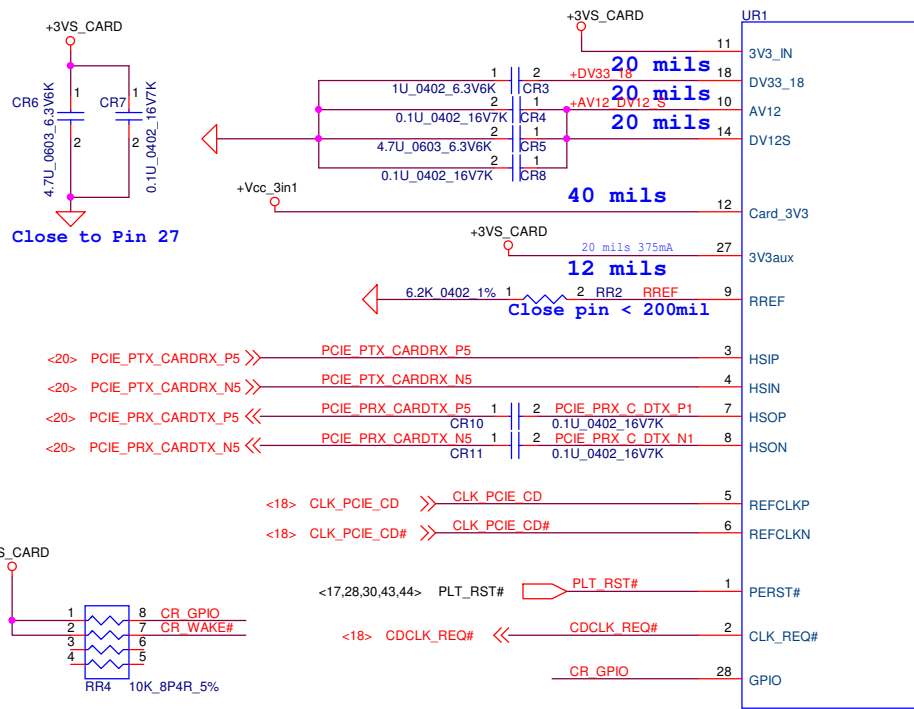
Port4, Gen3



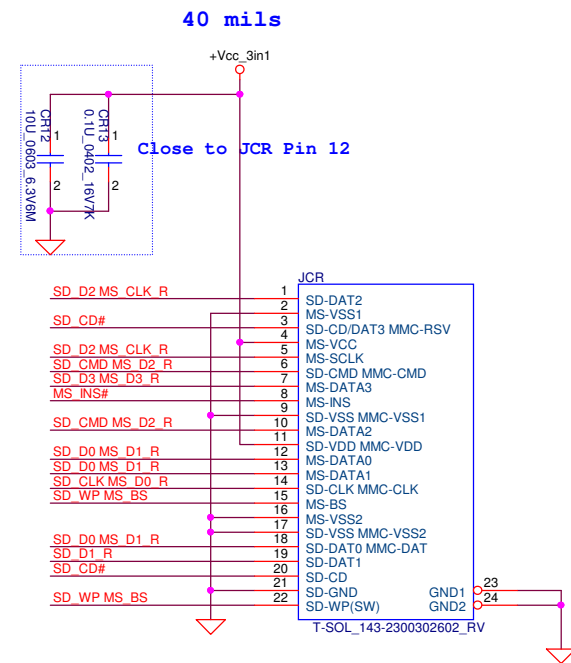
Port3, Gen2



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Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	Mini Card/LED
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				LA-B751P	
Date	Wednesday March 26 2014	Sheet	29 of 68	Rev	0.1



for project which need fine tune SD signal can change to R

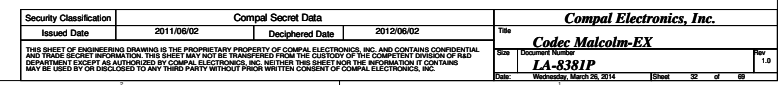


pin28:
If GPIO NO use for LED function and
GPIO must pull high

Internal Pull status

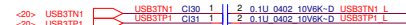
	NO Card	SD Insert	MS Insert
15_SP1	PD80	SD_D1_PU80	PD80
16_SP2	PD80	SD_D0_PU80	MS_D1_PD80
17_SP3	PD80	SD_CLK_PD80	MS_D0_PD80
19_SP4	PD80	SD_CMD_PU80	MS_D2_PD80
20_SP5	PD80	SD_D3_PU80	MS_D3_PD80
21_SP6	PD80	SD_D2_PU80	MS_CLK_PD80
29_SP7	PD200	SD_WP_PD200	MS_BS_PD200
30_SD_CD#	PU200	PU200	PU200
31_MS_CD#	PU200	PU200	PU200

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	Card Reader RTS5179
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				LA-B751P	Rev 0.1
				Date:	Wednesday, March 26, 2014
				Sheet	31 of 69

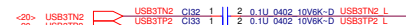
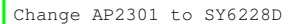


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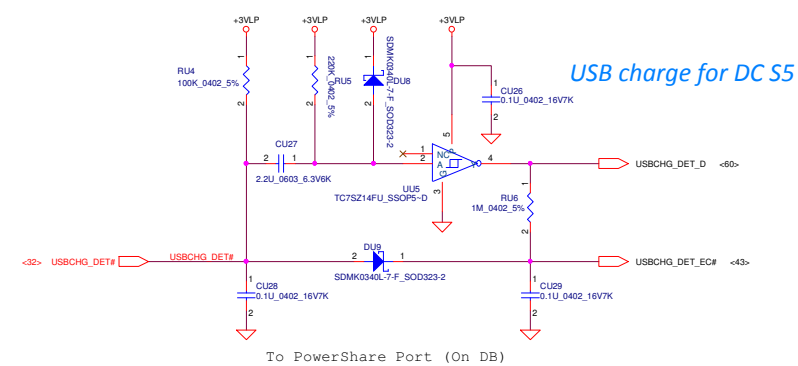
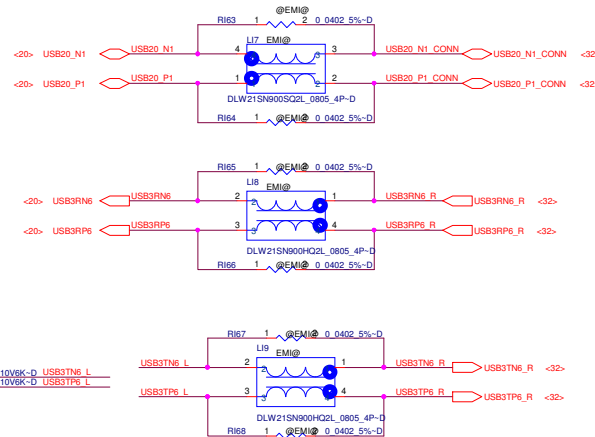
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Issued Date		2014/2/11	Deciphered Date	2014/2/11	
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				LA-B751P	
				Date: Wednesday, March 26, 2014	
				Sheet	33 of 69
				Rev	0.1



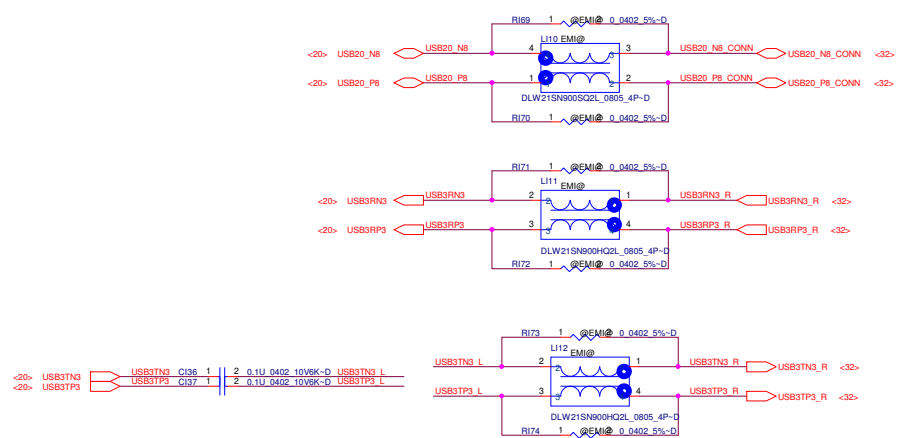
On MB (Right Side)



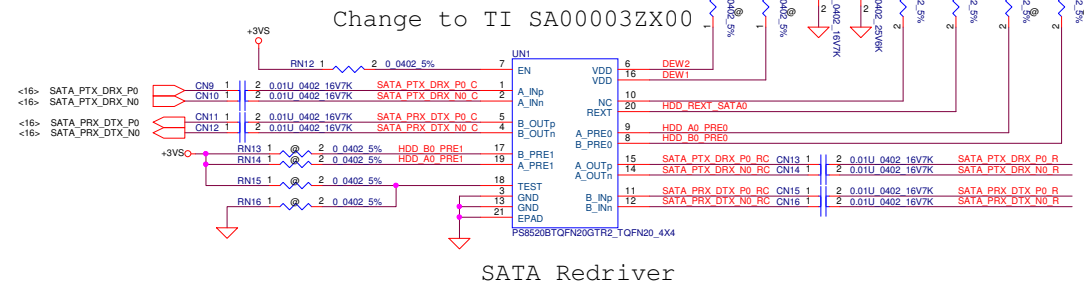
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	USB 3.0/2.0 x2 (left side)
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				LA-B751P	0.1
Date:	Wednesday, March 26, 2014		Sheet	34	of 69



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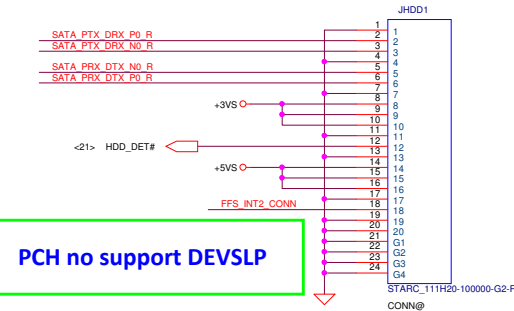
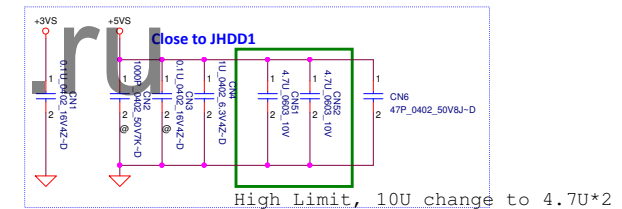
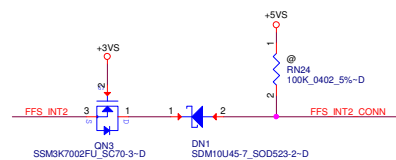
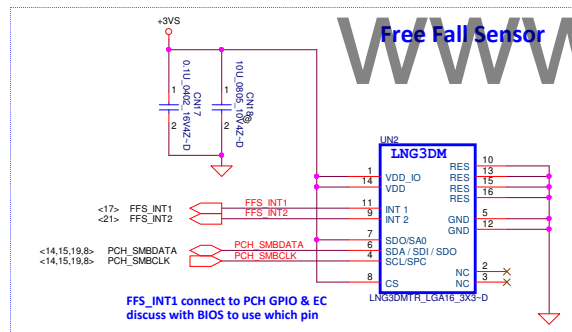
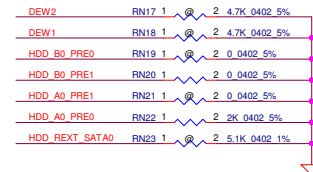


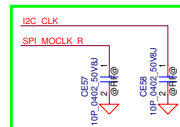
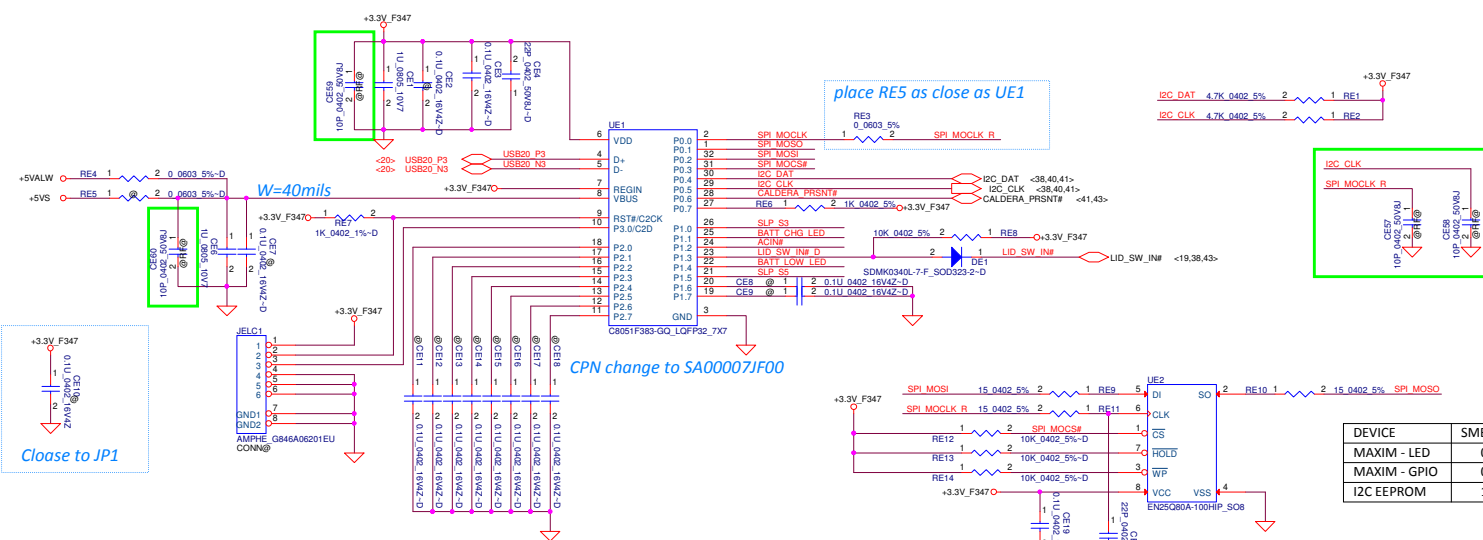
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	
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				LA-B751P	0.1
Date:		Wednesday, March 26, 2014		Sheet	35 of 69



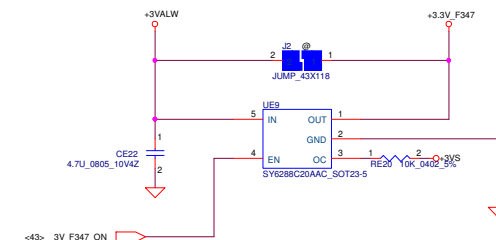
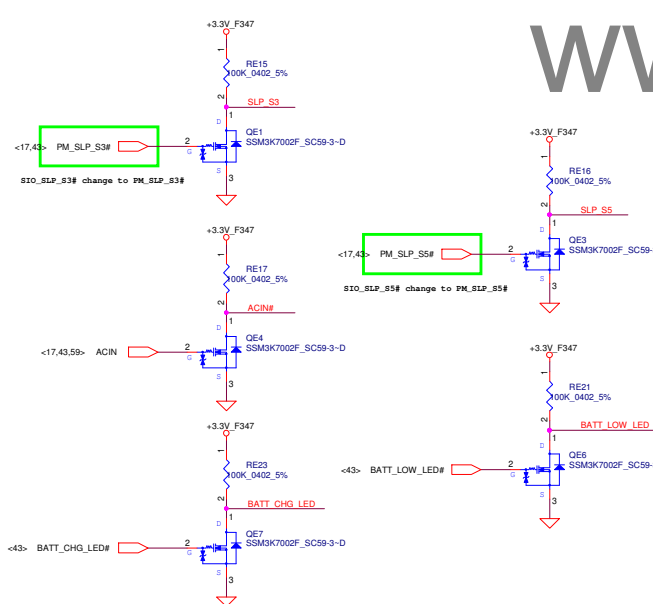
Pin 20:
PARADE PS8250B
Depop RS26
PERICOM PI3EQX6741ST
Pop RS26
ASMedia ASM1466
Pop RS26

Pin 9:
PARADE PS8250B
Depop RS24
PERICOM PI3EQX6741ST
Depop RS24
ASMedia ASM1466
Pop RS24 to pull down





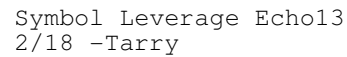
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



+3V_F347 behavior				
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BATT only	ON	ON	OFF	OFF

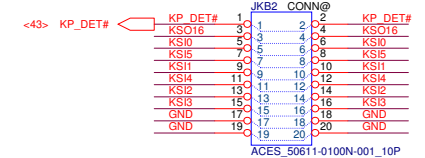
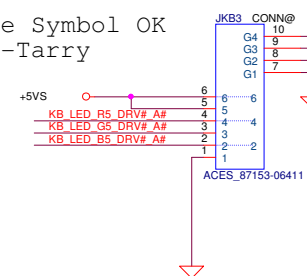
AC mode battery full in S5: turn off ELC controller

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[illegible]

Hot Key Conn. PWM

Hot Key Conn. Key Pad

**KB/HotKey conn**

LA-B751P

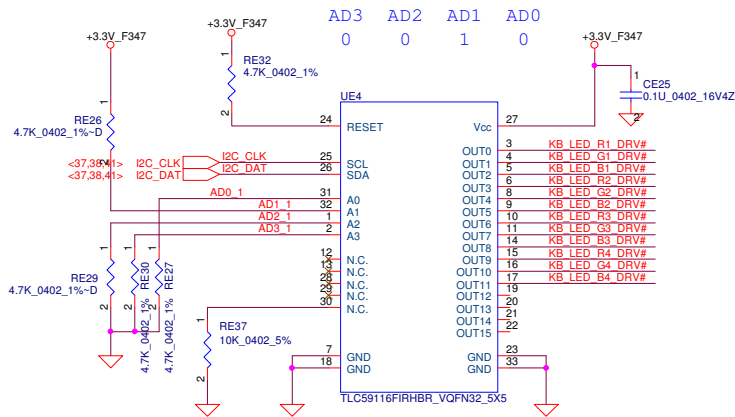
Date: Wednesday, March 26, 2014

Sheet 39 of 69

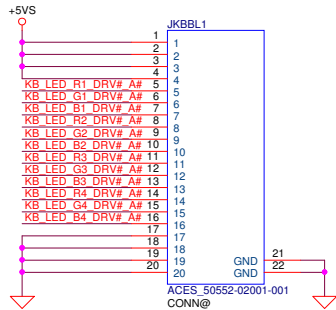
IV
0.1

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K/B Backlight



Check Pin define



KB BL LED

Symbol OK (Leverage Echo13)
2/18 -Tarry



DELL CONFIDENTIAL/PROPRIETARY

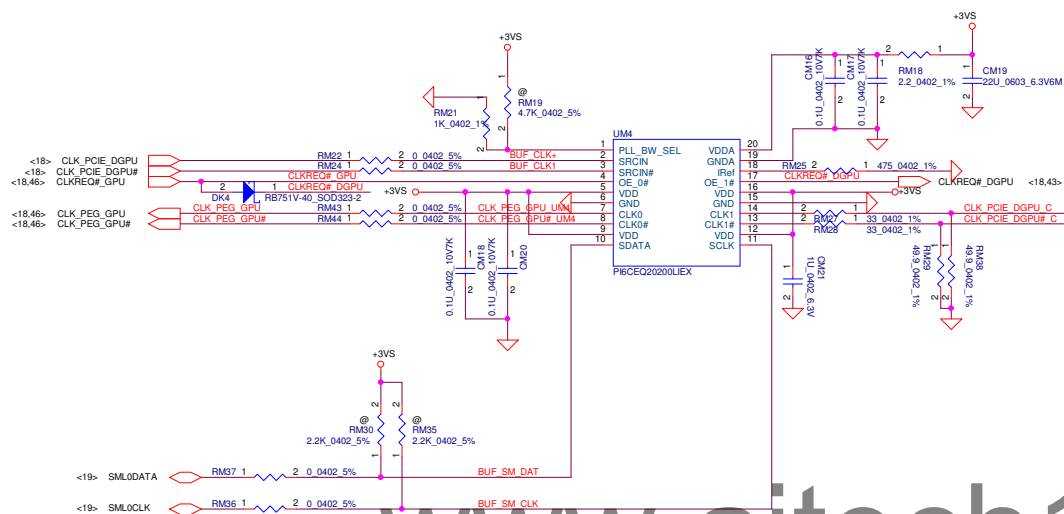


Compal Electronics, Inc.			
Title			
ELC(3)			
Size	Document Number	Rev	
	LA-B751P	0.1	
Date:	Wednesday, March 26, 2014	Sheet	40 of 69

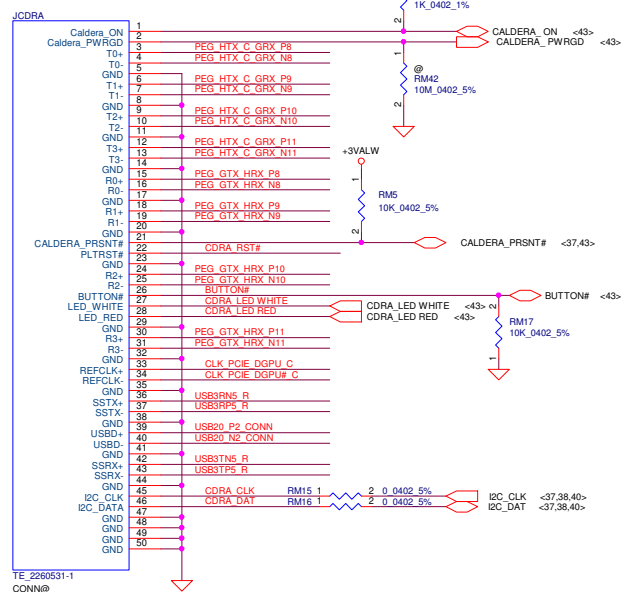
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EC控制/PIN
PCI_SMCLK
PCI_SMDAT
USB_PWR_EN#
DOCKING_LED ON#
DOCKING_LED OFF#
DOCK_PSID
DOCK_ACIN
DOCK_EN
PRSNT# R

PCIE_CLK_BUFFER

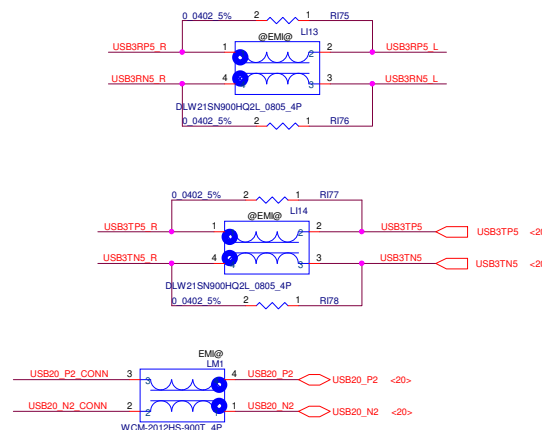


Caldera connector

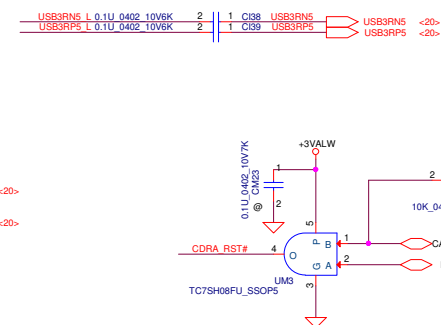


Symbol OK (Leverage Echo13)
2/18 -Tarry

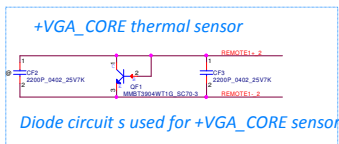
Diagram showing four input lines (two blue, two red) connected to a single output line labeled "Caldera". The inputs are labeled: PEG_HTX_C_GRX_P[8..11] <7>, PEG_HTX_C_GRX_N[8..11] <7>, PEG_GTX_HRX_P[8..11] <7>, and PEG_GTX_HRX_N[8..11] <7>.



Follow Echo 13 design.

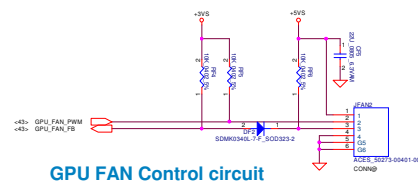
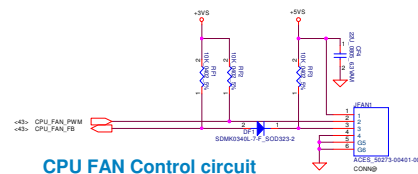
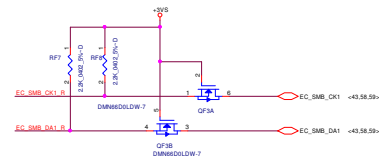
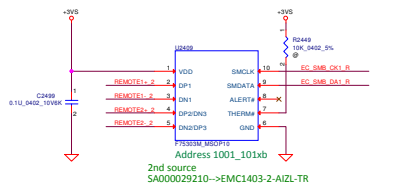
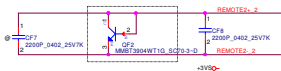


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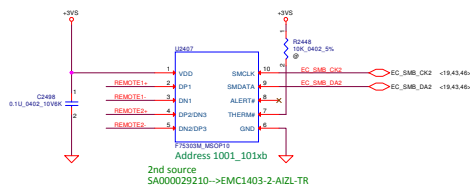


SKIN

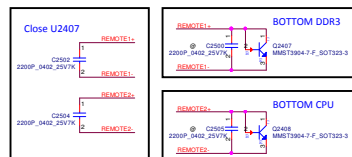
Diode circuit s used for skin temp sensor (placed around DIMM). Place C43 close to Q15as possible.



Fintek thermal sensor-> CPU core, DIMM

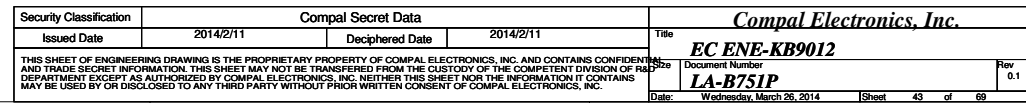


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REMOTEL2 (+/-):
Trace width/space:10/10 mil
Trace length:<8"

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FAN/TP/PWR SW				Rev
LA-B751P				Rev
Wednesday, March 26, 2014				Rev

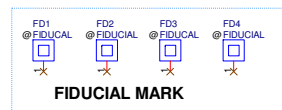


The diagram illustrates the connection between the TPM module and the AT97SC3205-TSSOP28-0. The TPM module is shown at the top, and the AT97SC3205-TSSOP28-0 is shown at the bottom. The connections are as follows:

- VCC to V_BAT
- GND to GND
- MISO to MISO
- MOSI to MOSI
- SPI_CLK to SPI_CLK
- SPI_CS# to SPI_CS#
- PLT_RST# to PLT_RST#
- TPM_IRQ# to TPM_IRQ#

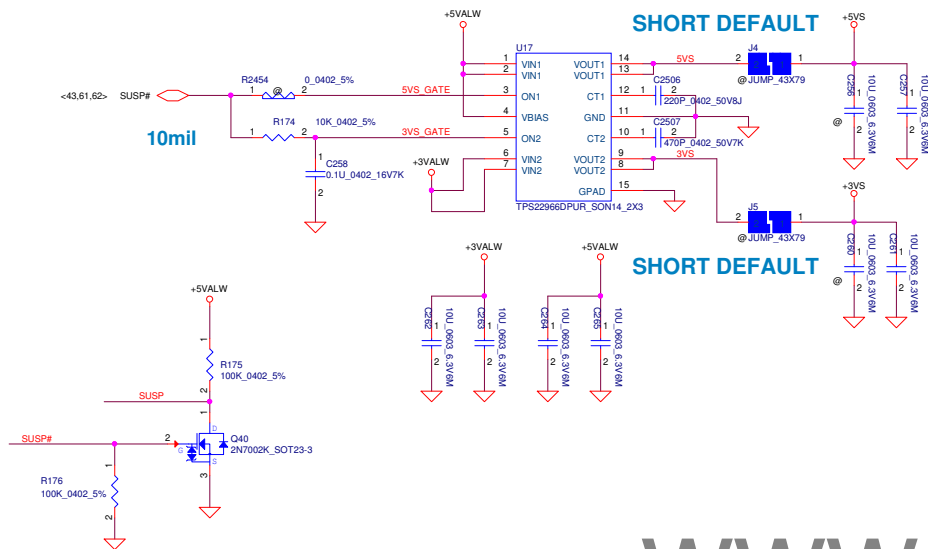
The TPM module also has a 33k pull-up resistor on the SPI_CLK line and a 33k pull-down resistor on the SPI_CS# line. The AT97SC3205-TSSOP28-0 has a 33k pull-up resistor on the SPI_CLK line and a 33k pull-down resistor on the SPI_CS# line.

Screw Hole



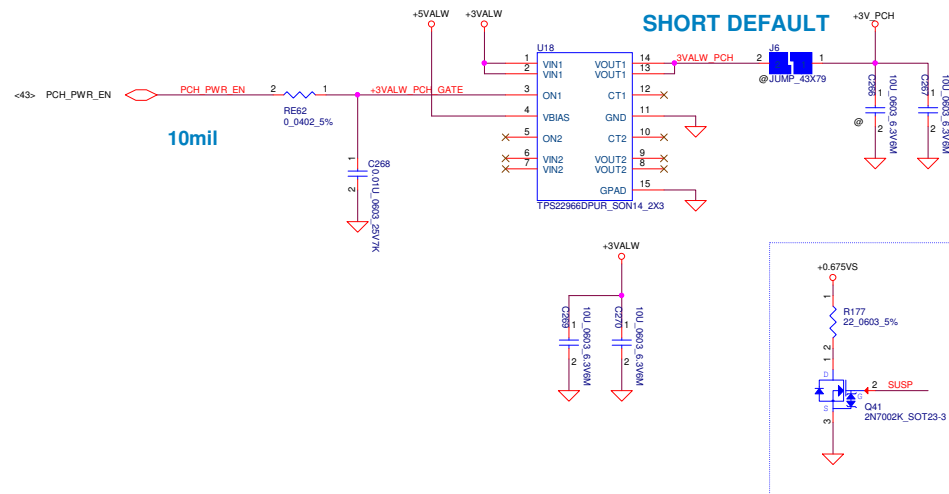
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	Screw Hole Document Number LA-B751P
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Date:	Wednesday, March 26, 2014			Sheet	44 of 69

+5VS and +3VS switch



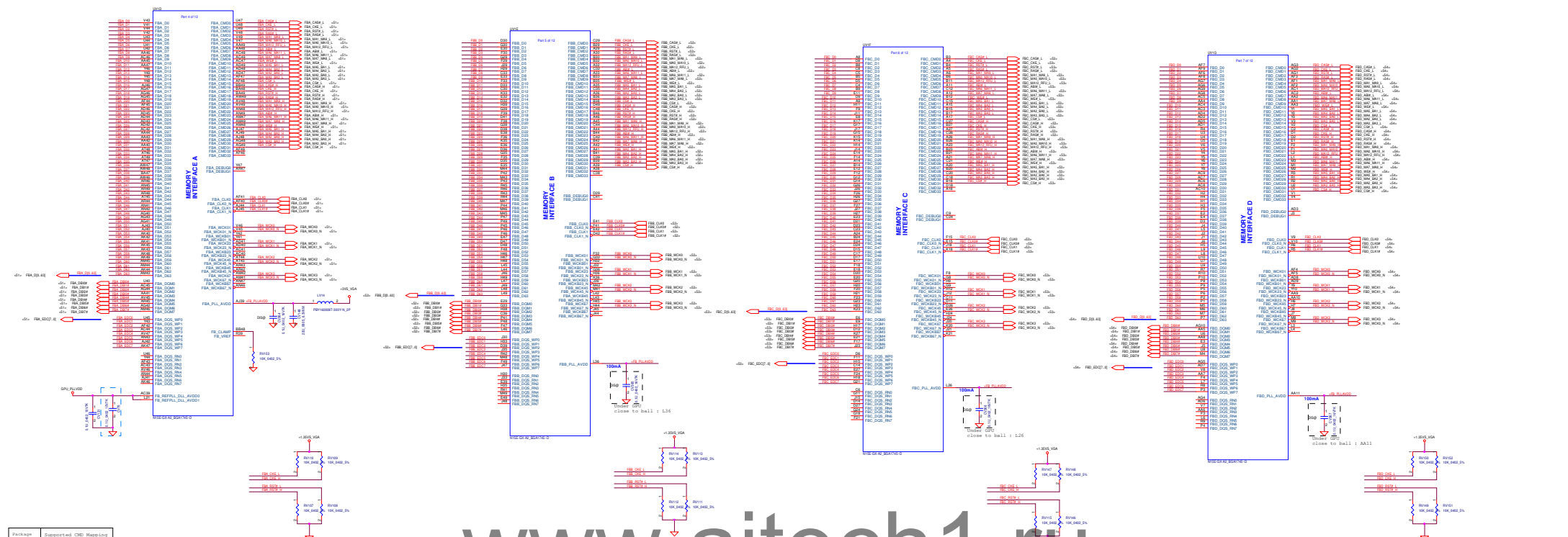
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+3VALW_PCH switch



For Intel S3 Power Reduction

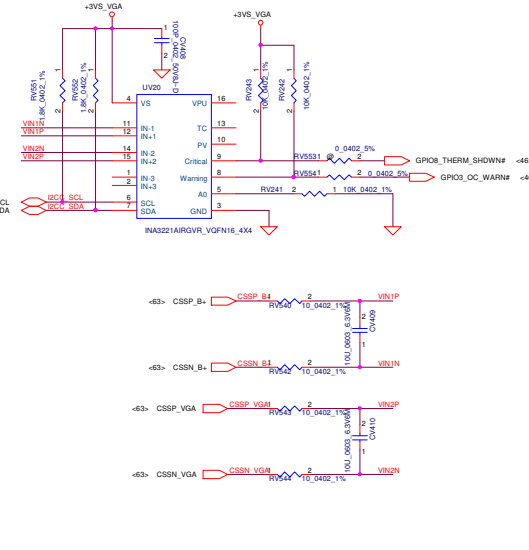
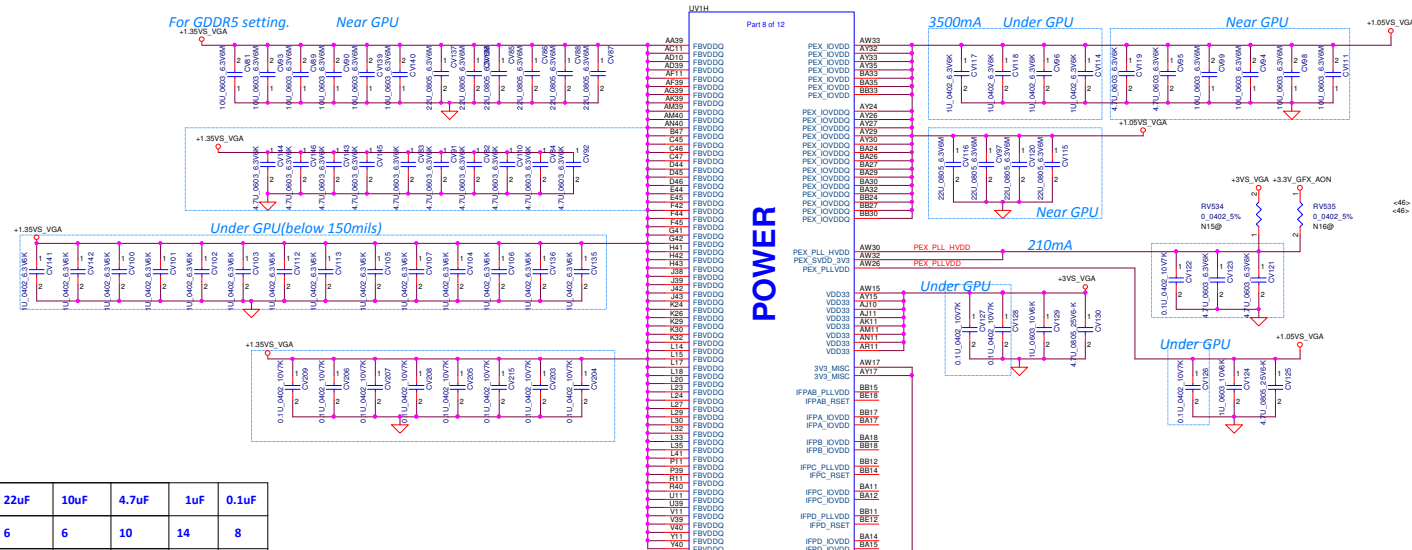
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Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	DC/DC Interface
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				Date	Wednesday, March 26, 2014
				Sheet	45 of 69
				Rev	0.1



Package	Supported CMC Mapping
QFN-44	
QFN-12	
QFN-20	

Node R Address	Node R Address	Node R Address
0...31	32...63	
CH01	CH02	CH03
CH04	CH05	CH06
CH07	CH08	CH09
CH10	CH11	CH12
CH13	CH14	CH15
CH16	CH17	CH18
CH19	CH20	CH21
CH22	CH23	CH24
CH25	CH26	CH27
CH28	CH29	CH30
CH31	CH32	CH33
CH34	CH35	CH36
CH37	CH38	CH39
CH40	CH41	CH42
CH43	CH44	CH45
CH46	CH47	CH48
CH49	CH50	CH51
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CH985	CH986	CH987
CH988	CH989	CH990
CH991	CH992	CH993
CH994	CH995	CH996
CH997	CH998	CH999
CH1000	CH1001	CH1002

Node F Address	Node F Address	Node F Address
0...31	32...63	
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CH04	CH05	CH06
CH07	CH08	CH09
CH10	CH11	CH12
CH13	CH14	CH15
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CH97	CH98	CH99



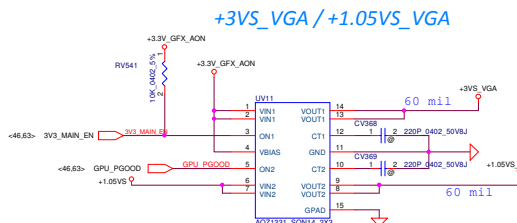
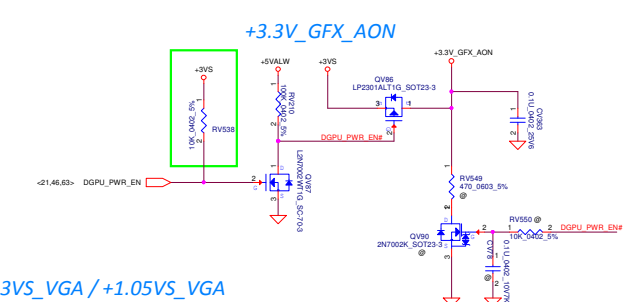
FBVDD/FBVDDQ (+1.35V_VGA)	22uF	10uF	4.7uF	1uF	0.1uF
GPU	6	6	10	14	8
Memory		2X8		4X8	10X8

	22uF	10uF	4.7uF	1uF	0.1uF
FBx_PLL_DLL_AVDD +GPU_PLLVDD(1.05)					
FBx_PLL_AVDD +FB_PLLAVDD(3.3)	1				1X4

	22uF	10uF	4.7uF	1uF	0.1uF
PEX_IOVDD/Q[1.05]	4	4	2	4	
PEX_PLLVDD[1.05]			1	1	1
PEX_SVDD_3V3 +3.3V_GFX_AON			2		1

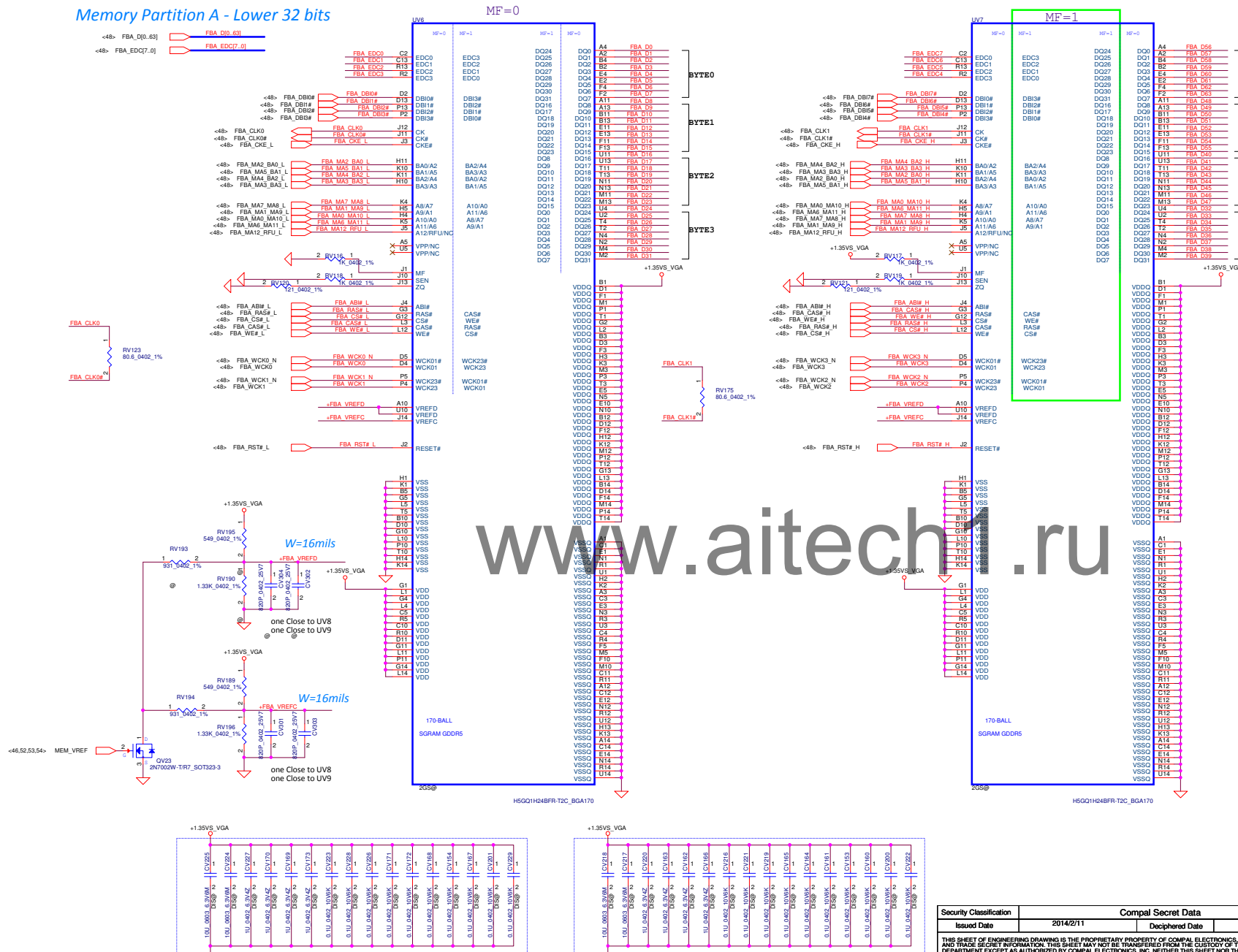
	22uF	10uF	4.7uF	1uF	0.1uF
3V3_Main +3V5_VGA			1	1	2
3V3_AON +3.3V_GFX_AON			1	1	1

1.05V	22uF	10uF	4.7uF	1uF	0.1uF
SP_PLLVDD VID_PLLVDD	1		1		1X2
GPU_PLLA VDD	1				5



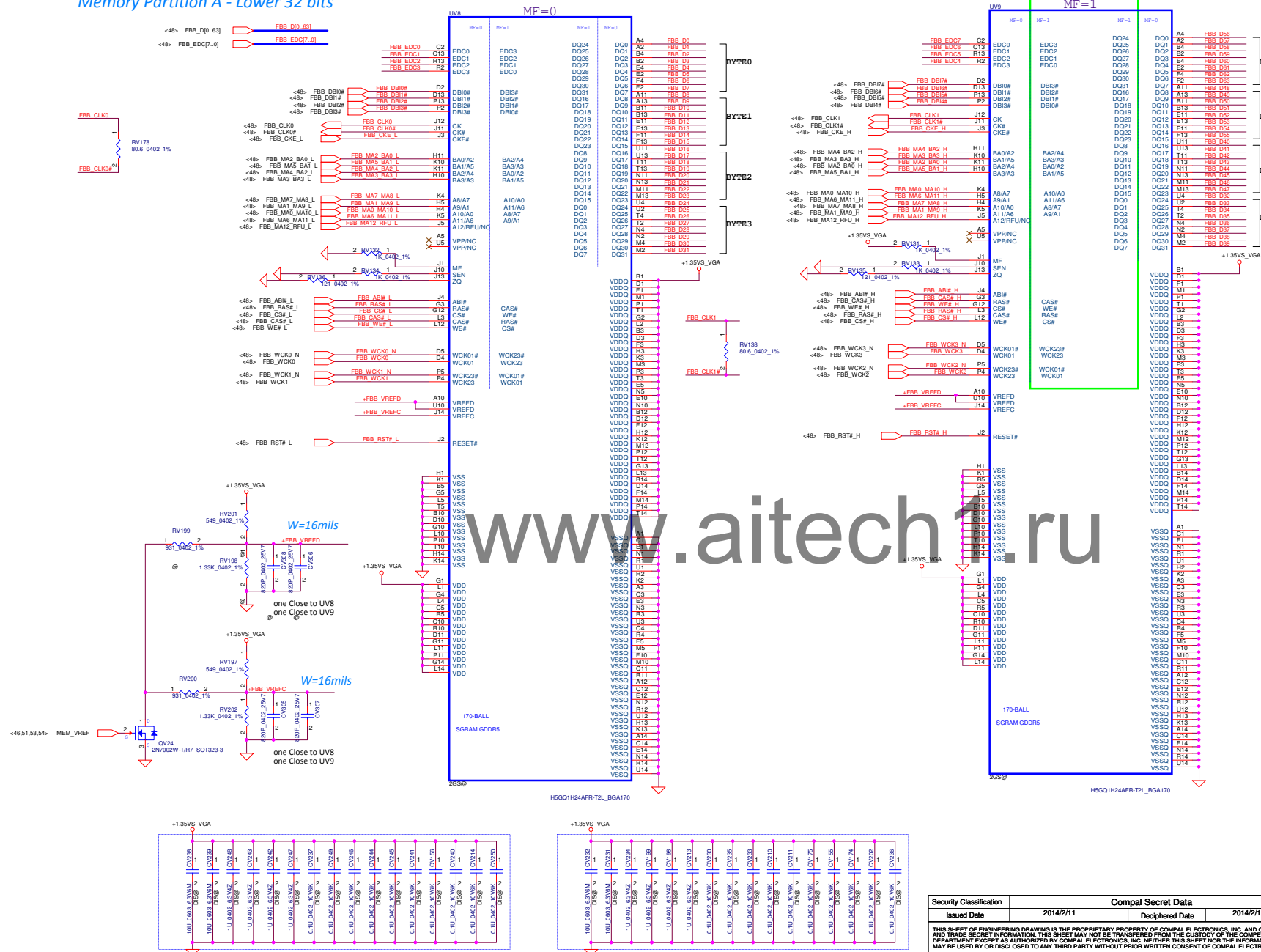
Security Classification	Compal Secret Data		Title
Issued Date	2014/2/11	Deciphered Date	2014/2/11
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS INFORMATION IS NOT TO BE DISCLOSED OR USED BY ANY OTHER DIVISION OF RADA DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			<p>NISP-GX (115) PEG & DAC</p> <p>Size Contour LA-8751P</p>
Date	Wednesday, March 26, 2014	Sheet	48 of 69

Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Compal Electronics, Inc. N1SP GDDR5 A Lower LA-B751P
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			Rev	0.1
Date:	Wednesday, March 26, 2014	Time	5:14	PM

Memory Partition A - Lower 32 bits



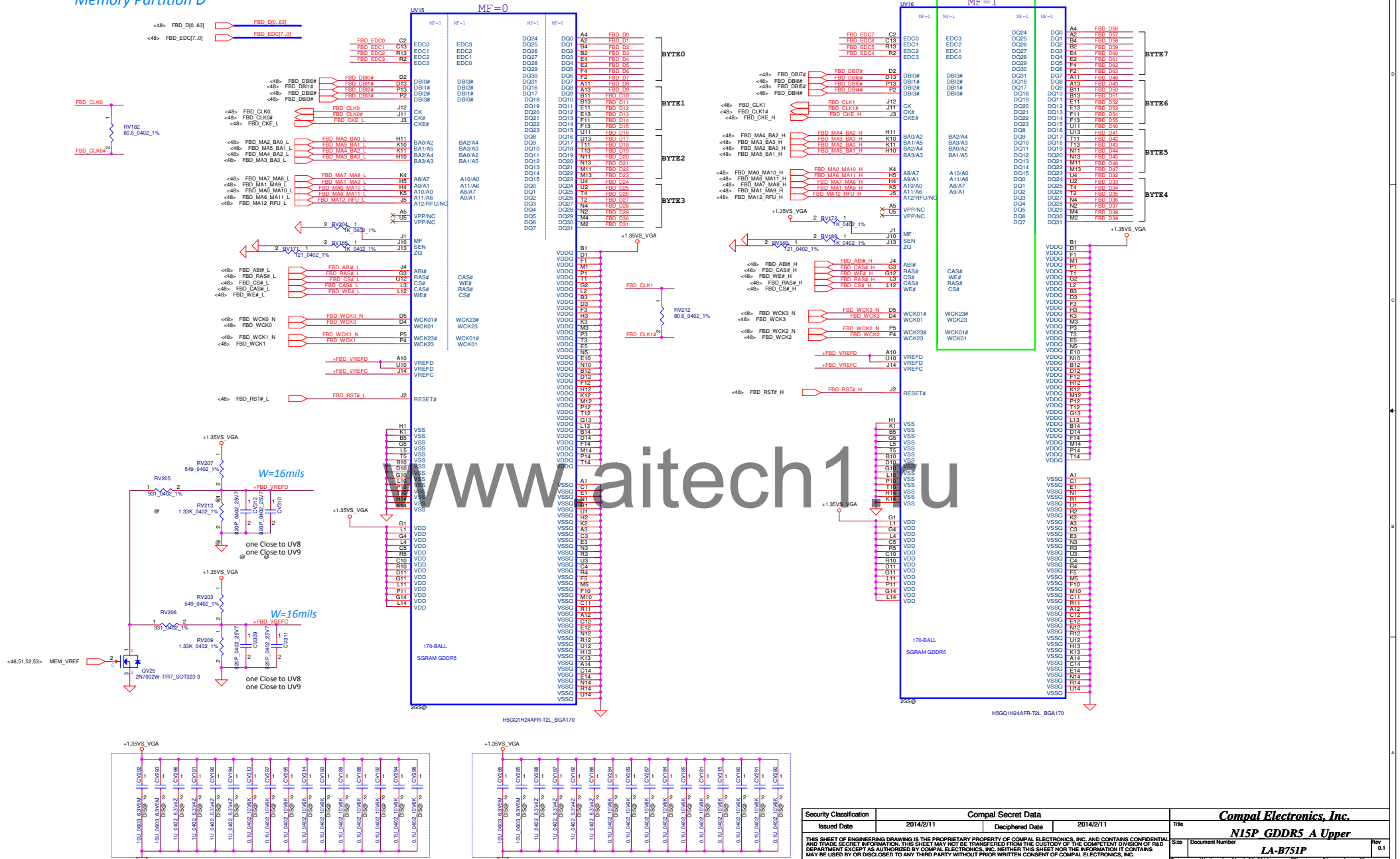
Security Classification	Compal Secret Data		Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Compal Electronics, Inc.
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Size	Document Number		Rev	
	LA-B751P		0.1	
Date:	Wednesday, March 26, 2014		Sheet	52 of 69

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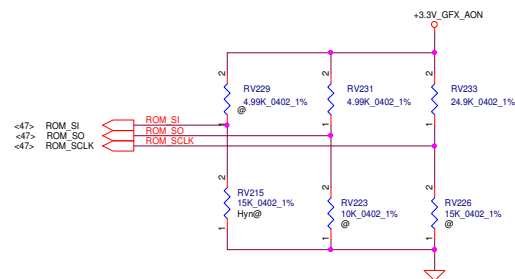
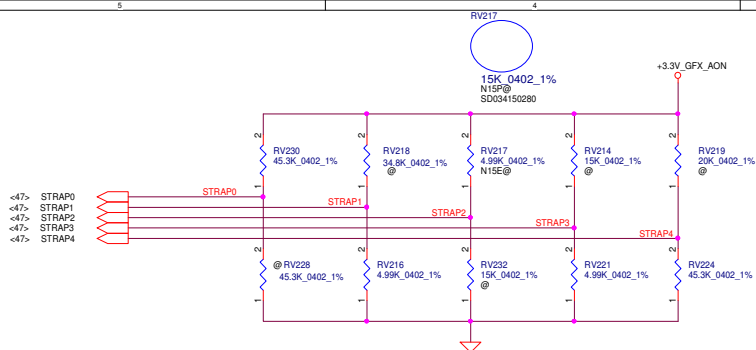


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Memory Partition D



Security Classification	Compal Secret Data			Title			Compal Electronics, Inc.		
Issued Date	2014/2/11	Deciphered Date	2014/2/11	N15P GDDR5 A Upper					
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				LA-B751P			0.1		
				Date:	Wednesday, March 26, 2014	ISheet	54	of	69



R_pu



VRAM	Strap	ROM-SI
Hynix H5GC4H24MFR-T2C	0x2	PL 15K
Samsung K4G41325FC-HC04	0x3	PL 20K

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[4]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHNAGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	PU to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

PCI_DEVID

SUB_VENDER
0- w/o dGPU ROM
1-w/ dGPU ROM

FB[1:0]
0-Reserved
1-Reserved
2-256M
3-Reserved

VGA_DEVICE
0- Non-permyary 3D
1-

SMB_ALT_ADDR
0-0x9E
1-0x9C(Multi-GPU)

PEX_PLL_EN_TERM
0-Disable
1-Enable

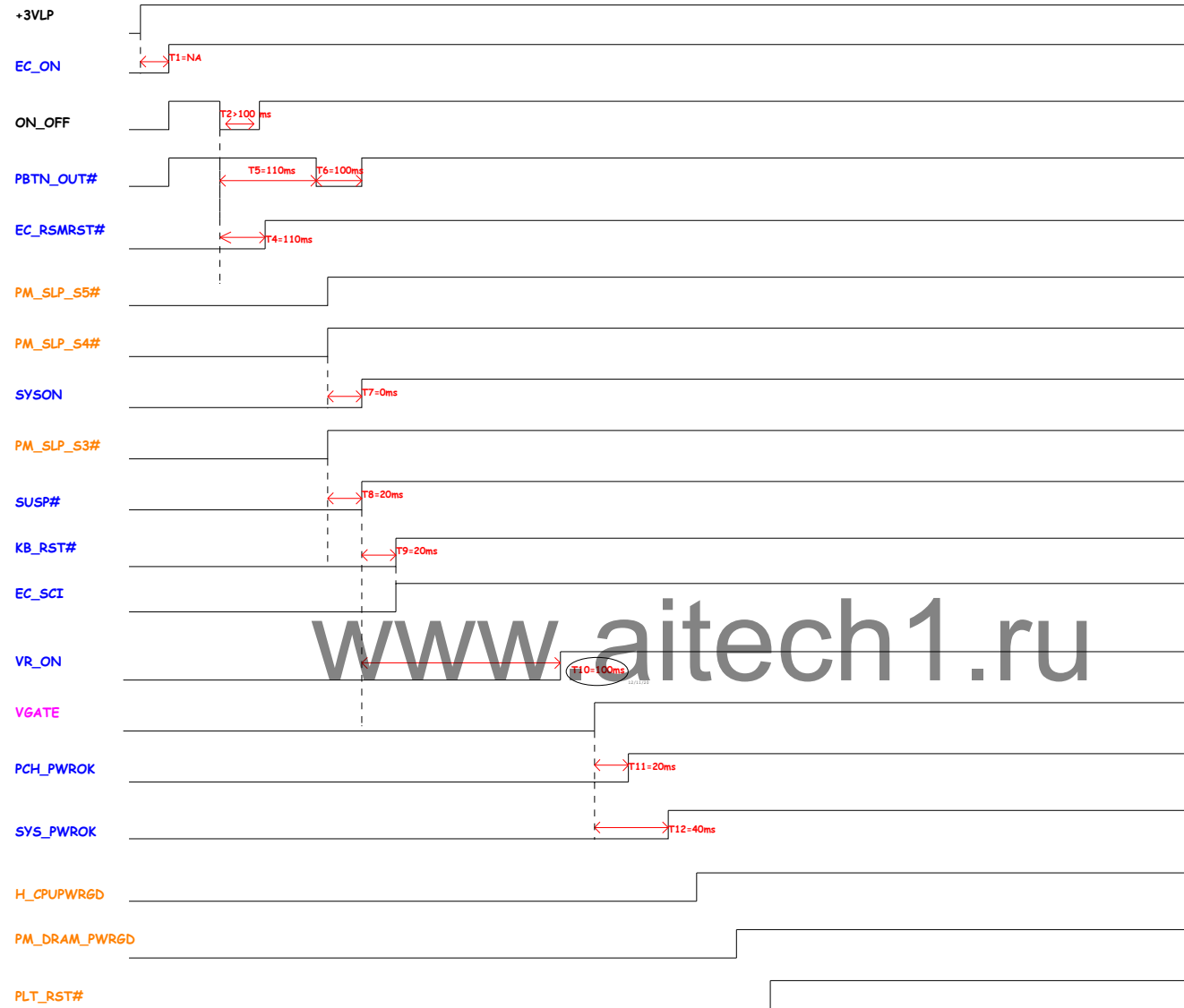
3GIO_PADCFG
0110-GEN1/GEN2
0000-GEN3

PCIE_MAX_SPEED
0-booting to PCIE Gen1
1-booting to PCIE Gen2/Gen3

PCIE_SPEED_CHNAGE_GEN3
0-Disable PCIE Gen3
1-Enable PCIE Gen3

Security Classification	Compal Secret Data			Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	NISP-GX (1/5) PEG & DAC	
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				Sheet	55 of 69
				Rev	0.1

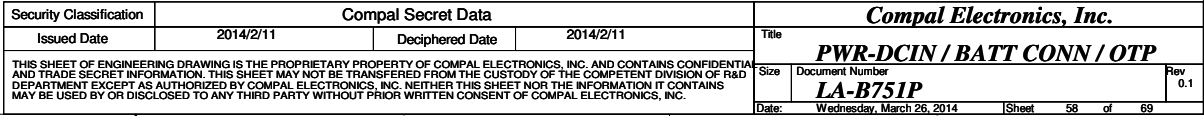
Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
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41							

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CC = 3A
CV = 17.7V

I_{ada}=0~12.3A (240W)
I_{ada}=0~9.23A (180W)

ADP_I = 40*I_{adapter}*R_{sense}

BATT++

VIN

BAT54CW_SOT323-3

PC707

PC708

PC709

PC710

PC711

PC712

PC713

PC714

PC715

PC716

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PC989

$$3.07A + 4.17A = 7.24A$$

EM@ PL100
U1H 6.6A 20% 5X5X3 M
3.5V B+
U1U 0402 25V6
EM@ PC103
220P 0402 3V7K
PC104
10U 0805 25V6K
PC113
10U 0805 25V6K

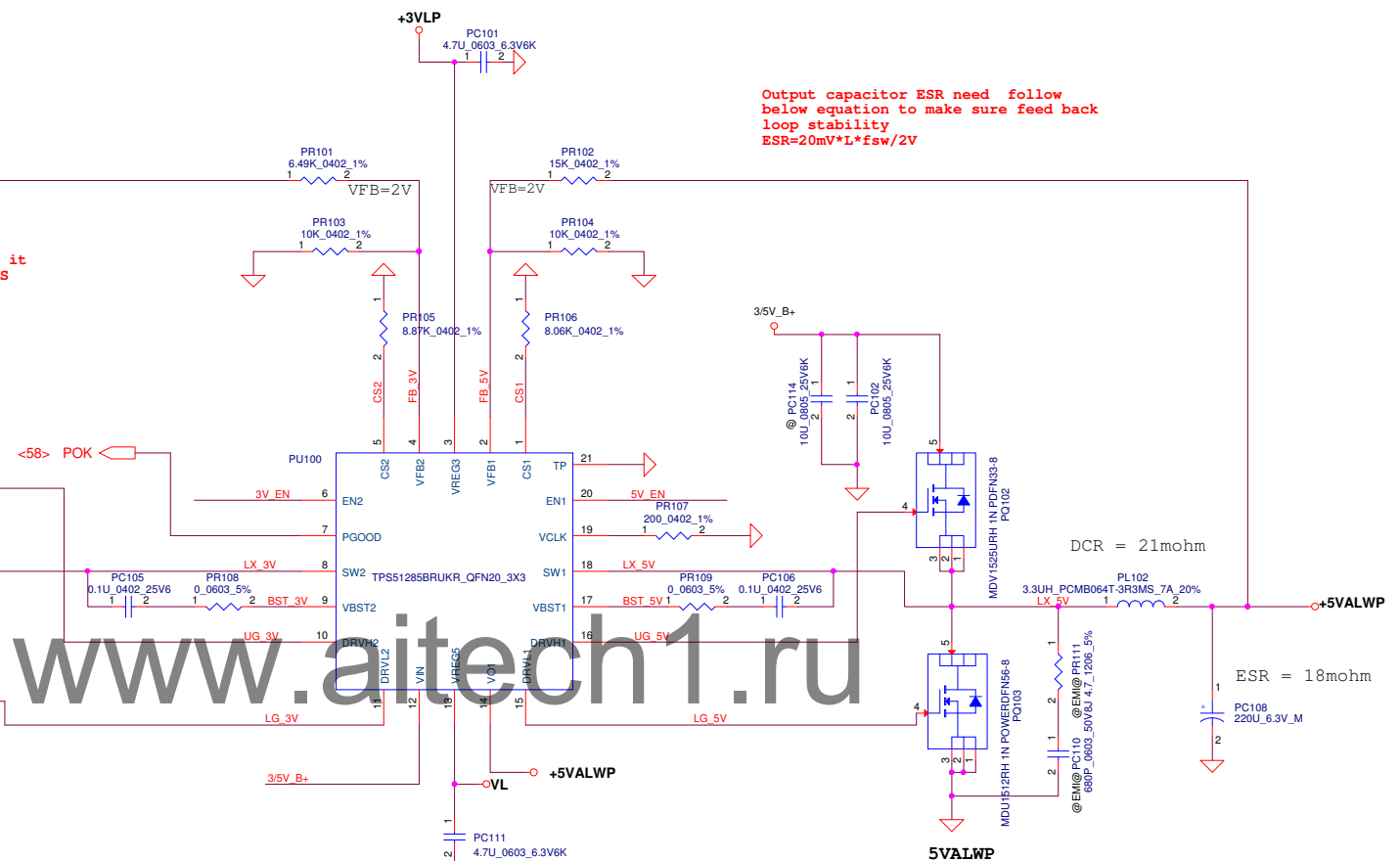
+3VALWP

ESR = 18mohm

S COIL 2.2u

	TYP	MAX
H/S Rds (on) :	11.5mohm	14mohm
L/S Rds (on) :	4.2mohm	5mohm

	TYP	MAX
H/S Rds (on) :	11.5mohm	14mohm
L/S Rds (on) :	4.2mohm	5mohm

[illegible]

5VALWP
TDC=7.8A
Peak Current 11.2A
OCP current 13.4A
FSW=400kHz

	TYP	MAX
H/S Rds (on) :	11.5mohm	14mohm
L/S Rds (on) :	4.2mohm	5mohm



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Date: Wednesday, March 26, 2014				Sheet 60 of 69		

$$1.35V \times (7.64A + 1A) = 11.66W$$

$$11.66 / 0.85 / 11 = 1.24A$$

1.35VP
TDC=7.64A
Ipeak=10.92A
OCP=13.1A
Switching Frequency: 285kHz

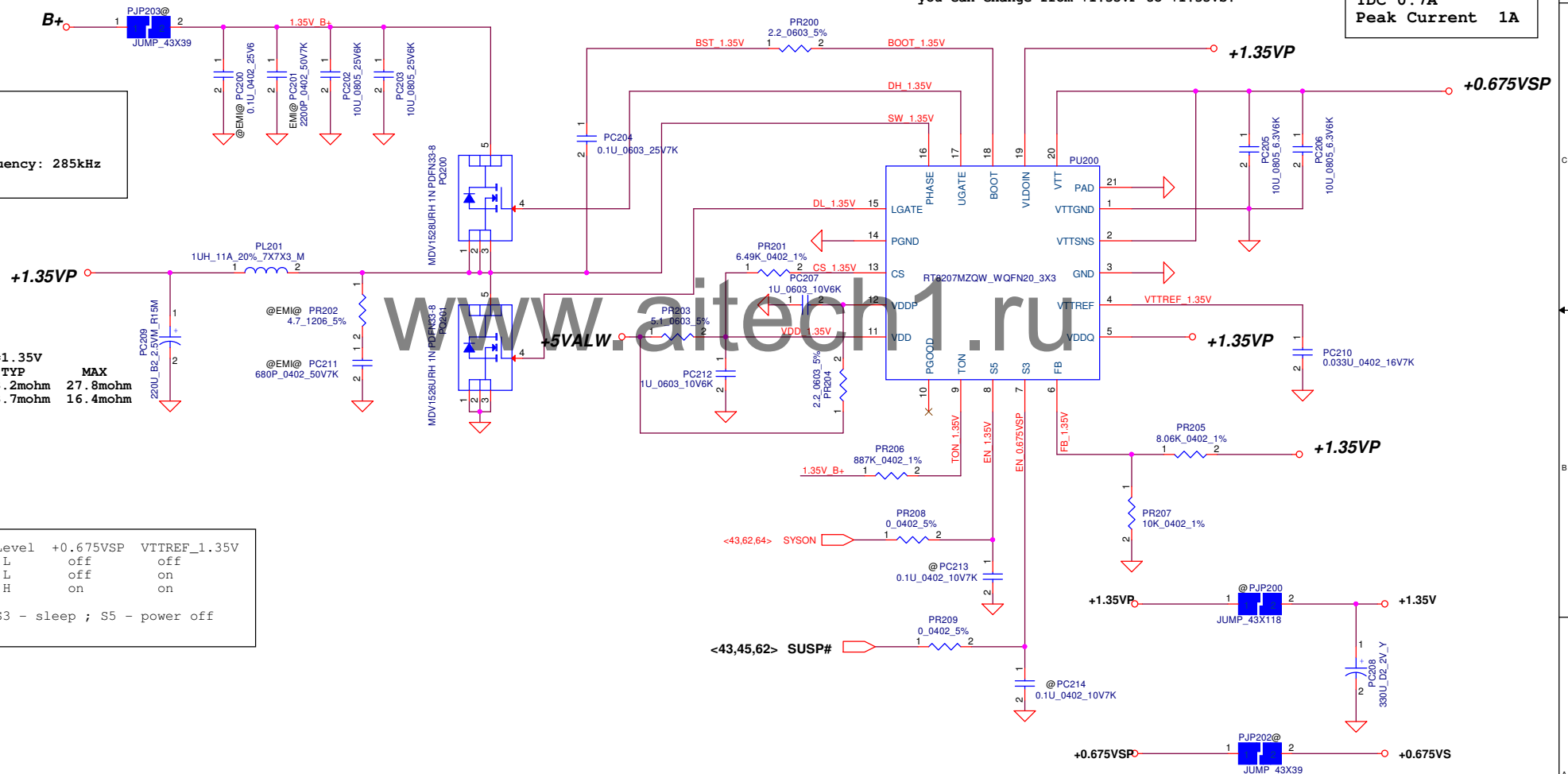
OVP: 110%~120%
VFB=0.75V, Vout=1.35V
TYP
H/S Rds(on) : 23.2mohm 27.8mohm
L/S Rds(on) : 13.7mohm 16.4mohm
MAX

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

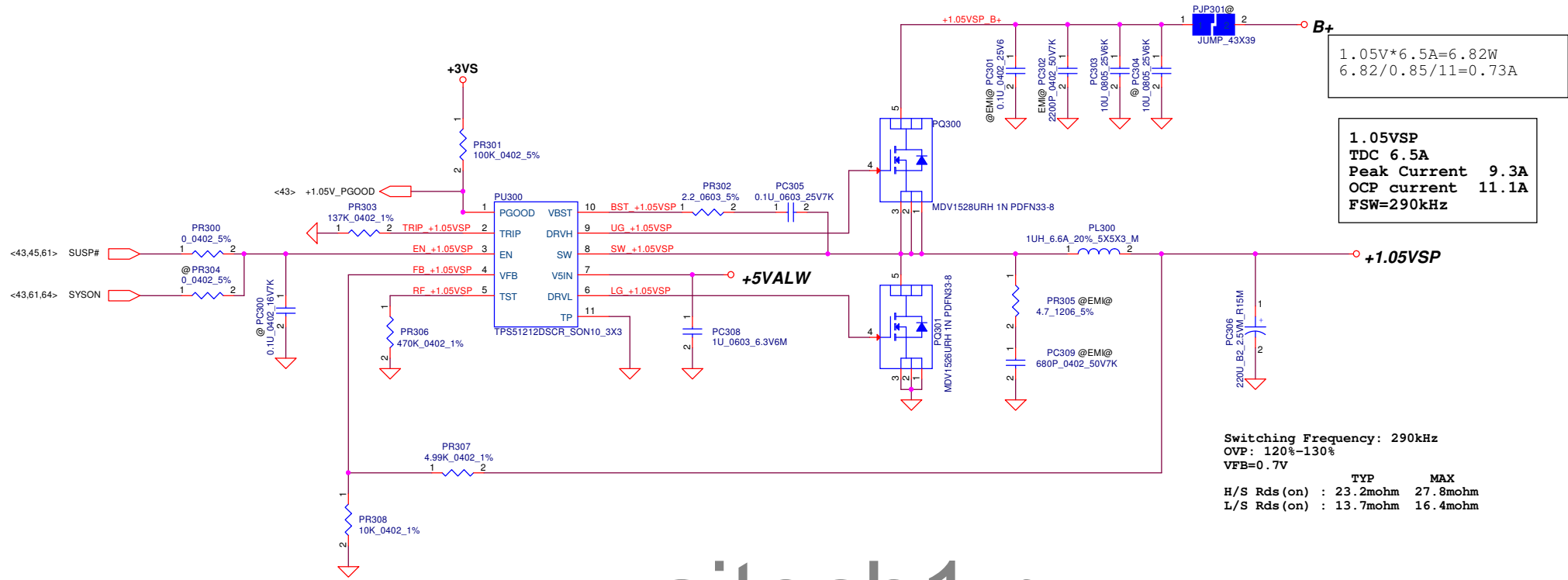
Note: S3 - sleep ; S5 - power off

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675VOLT +/- 5%
TDC 0.7A
Peak Current 1A



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Size	Document Number	Rev		LA-B751P	
Date	Wednesday, March 26, 2014	Sheet	61	of	69



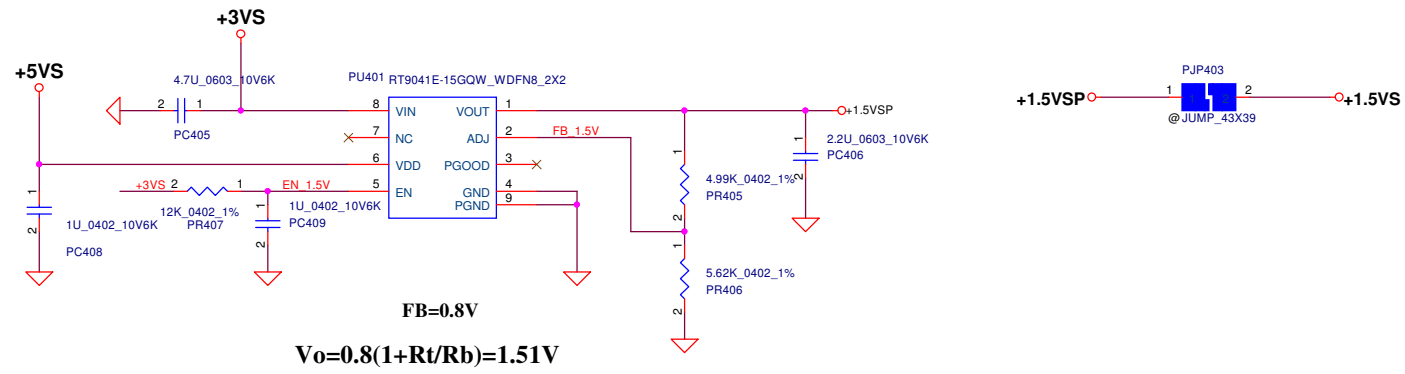
$$1.05V \times 6.5A = 6.82W$$

$$6.82 / 0.85 / 11 = 0.73A$$

1.05VSP
TDC 6.5A
Peak Current 9.3A
OCF current 11.1A
FSW=290kHz

Switching Frequency: 290kHz
OVP: 120%-130%
VFB=0.7V

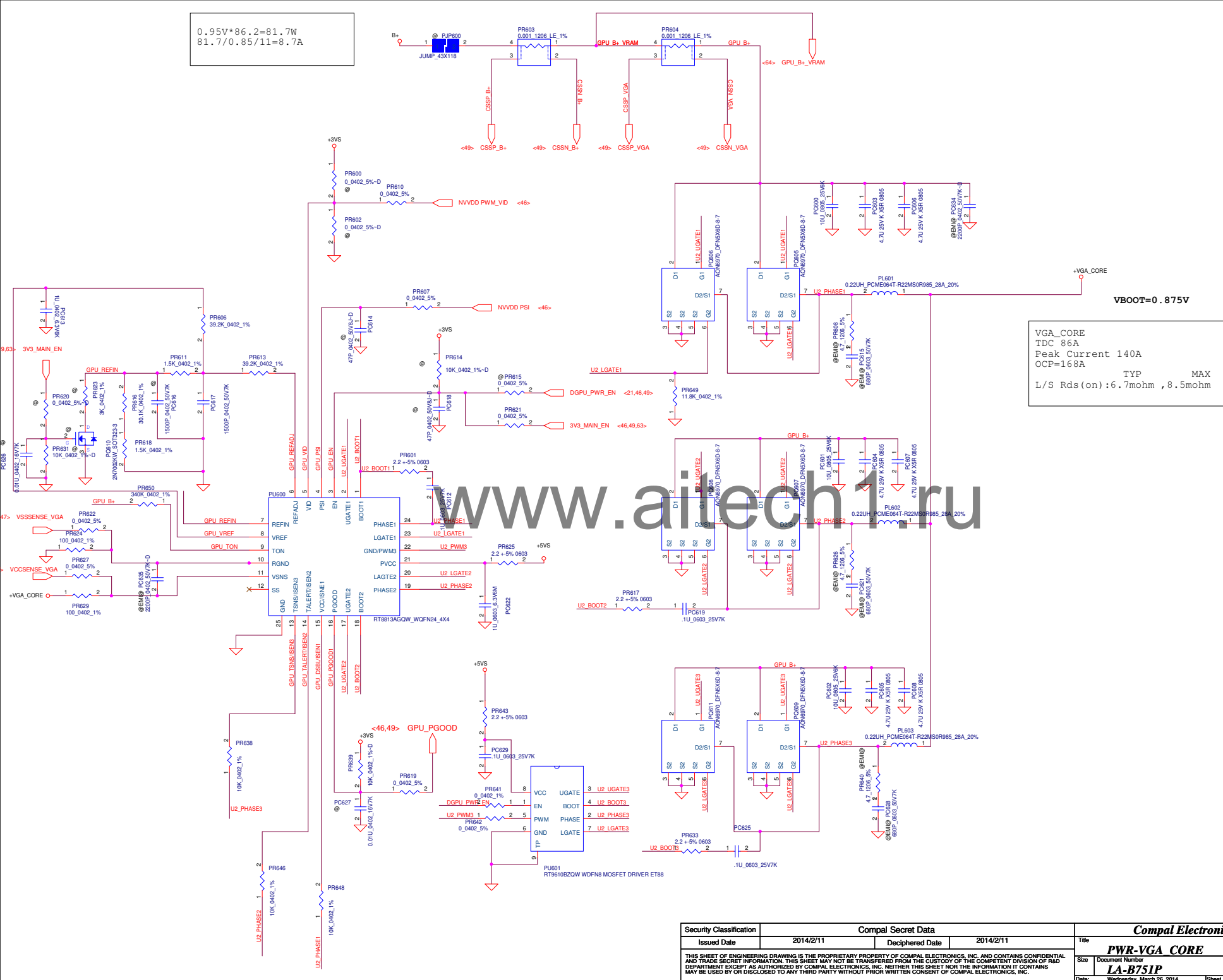
	TYP	MAX
H/S Rds (on)	23.2mohm	27.8mohm
L/S Rds (on)	13.7mohm	16.4mohm



$$V_o = 0.8(1 + R_t/R_b) = 1.51V$$

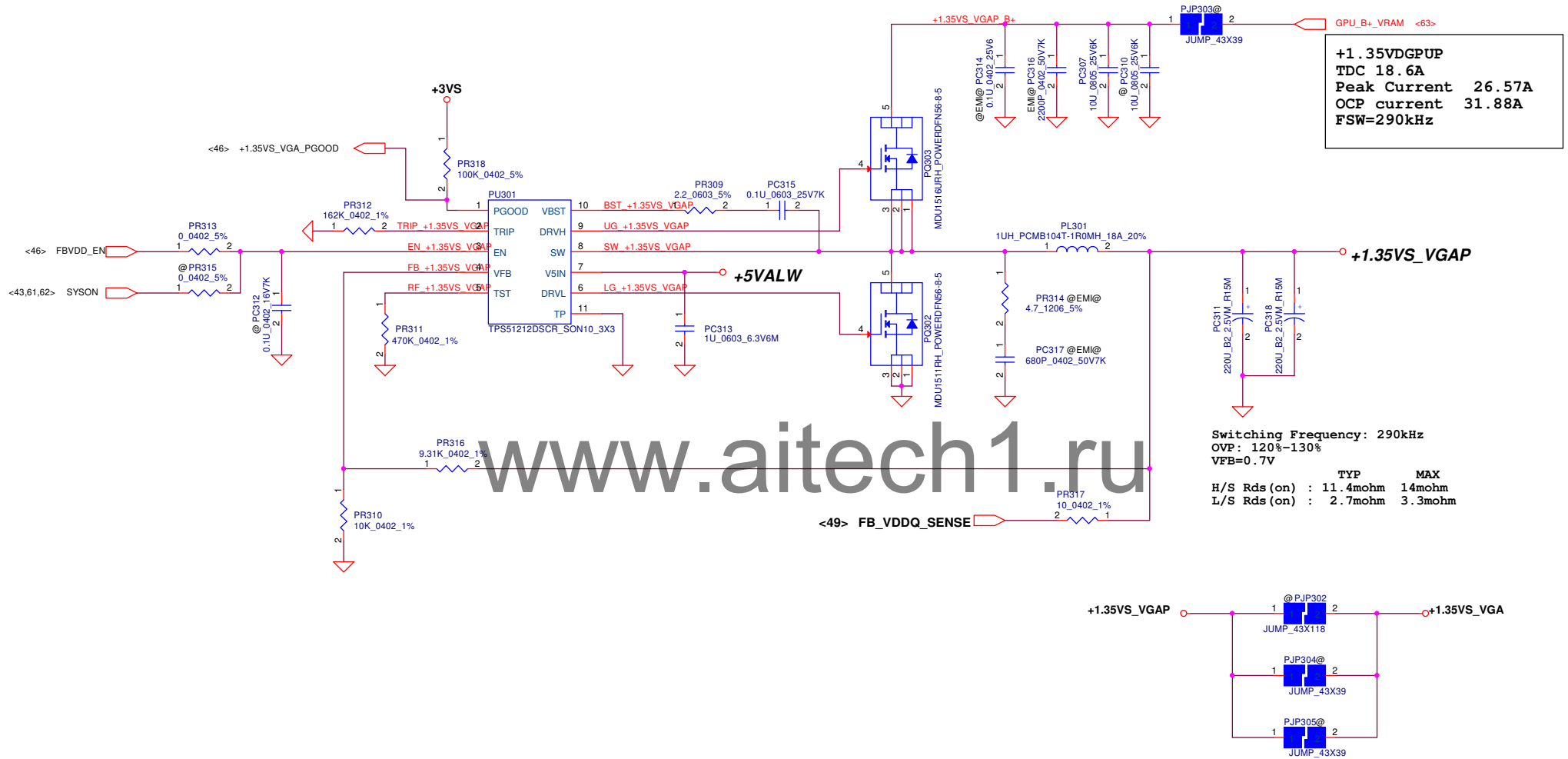
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Size	Document Number	Rev		LA-B751P	
Date:	Wednesday, March 26, 2014	Sheet	62	of	69

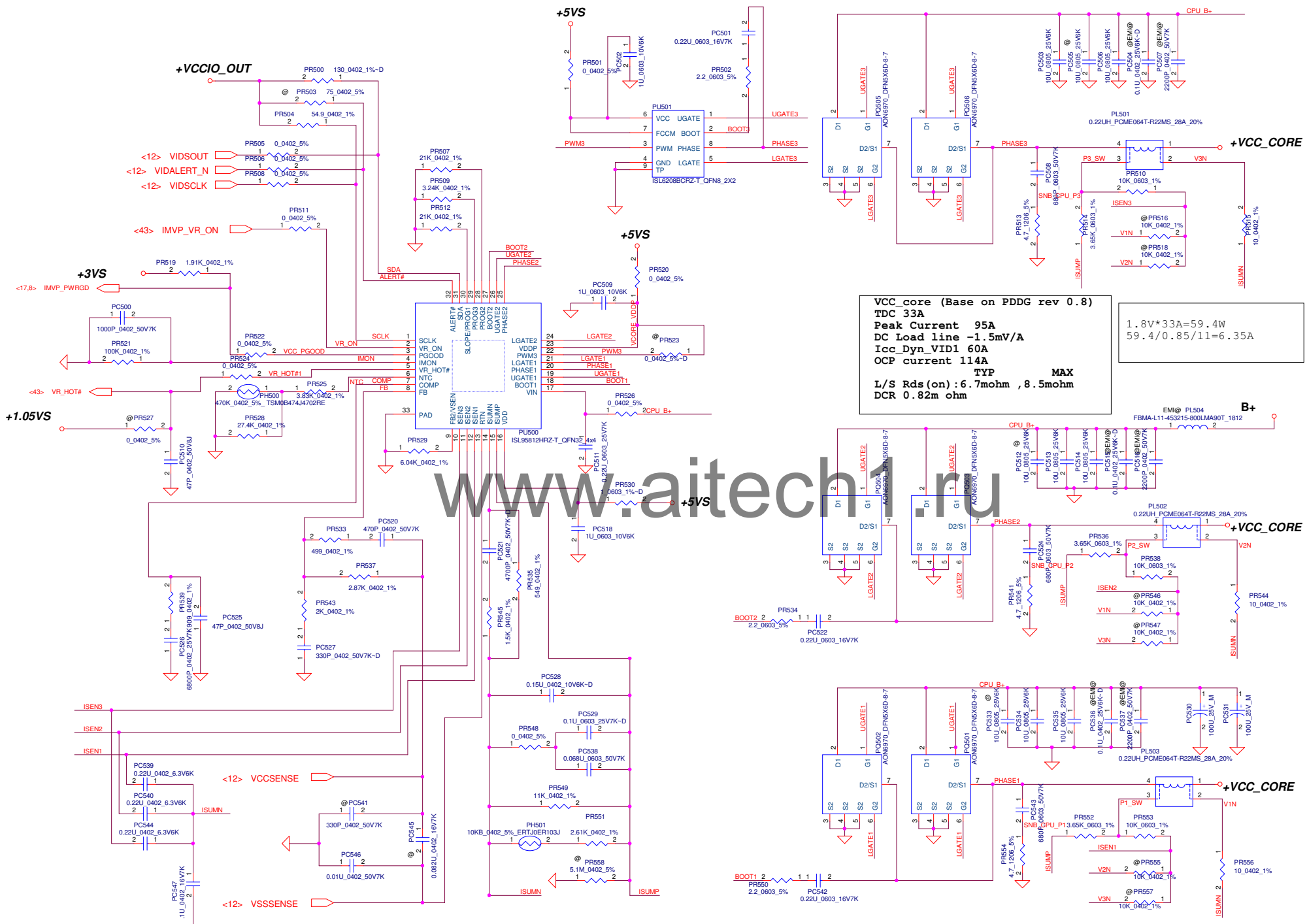
$$0.95V \cdot 86.2 = 81.7W$$
$$81.7 / 0.85 / 11 = 8.7A$$



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			Size	Rev
			Dwg. No. 2014	0.1
			Sheet 69 of 69	

1.35V*18.6A=25.11W
33.42/0.85/11=2.68A



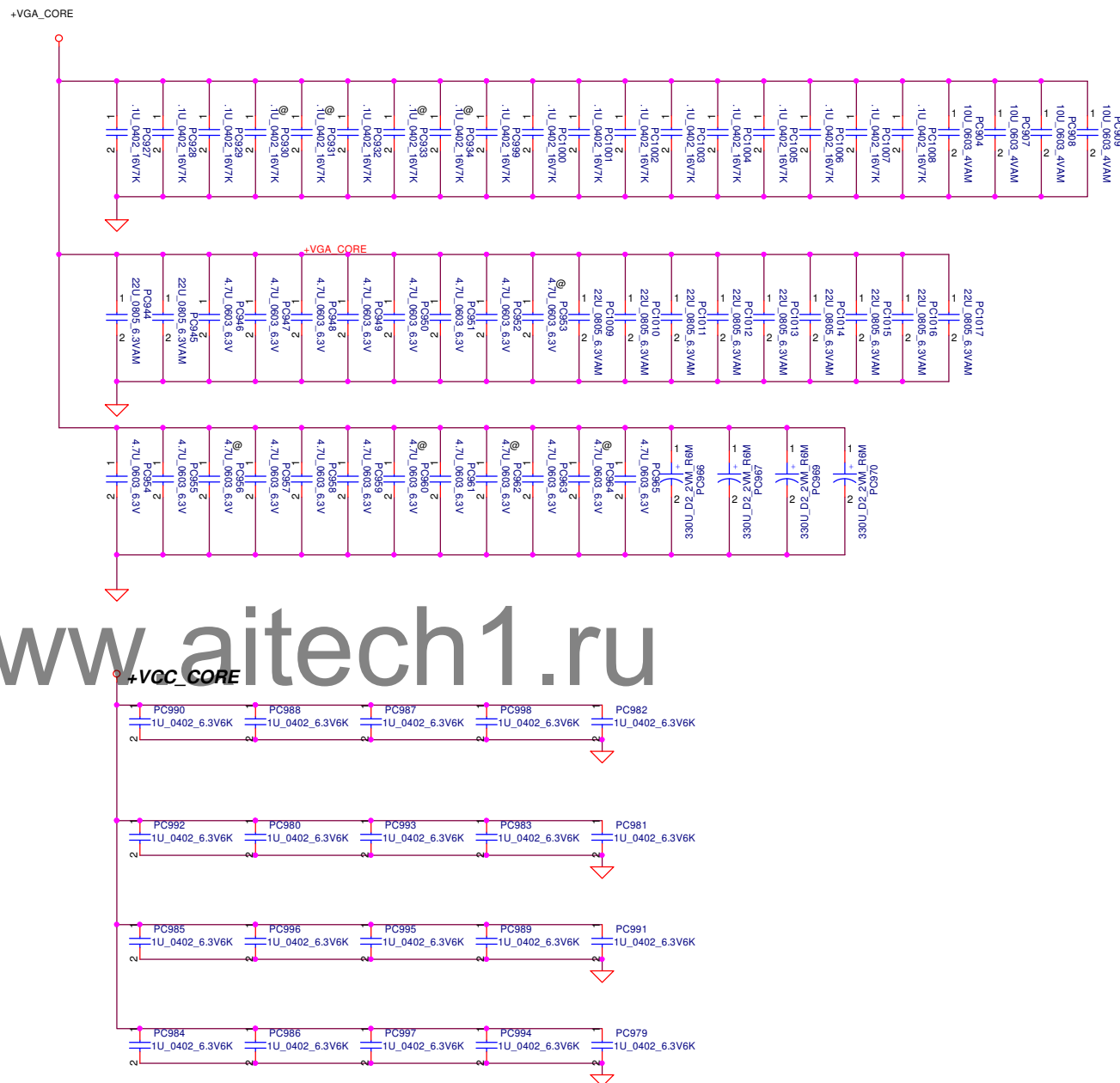


VCC_core (Base on PDDG rev 0.8)
TDC 33A
Peak Current 95A
DC Load line -1.5mV/A
Icc_VID1D 60A
OCP current 114A
TYP MAX
L/S Rds(on) : 6.7mohm , 8.5mohm
DCR 0.82m ohm

$1.8V \times 33A = 59.4W$
 $59.4 / 0.85 / 11 = 6.35A$

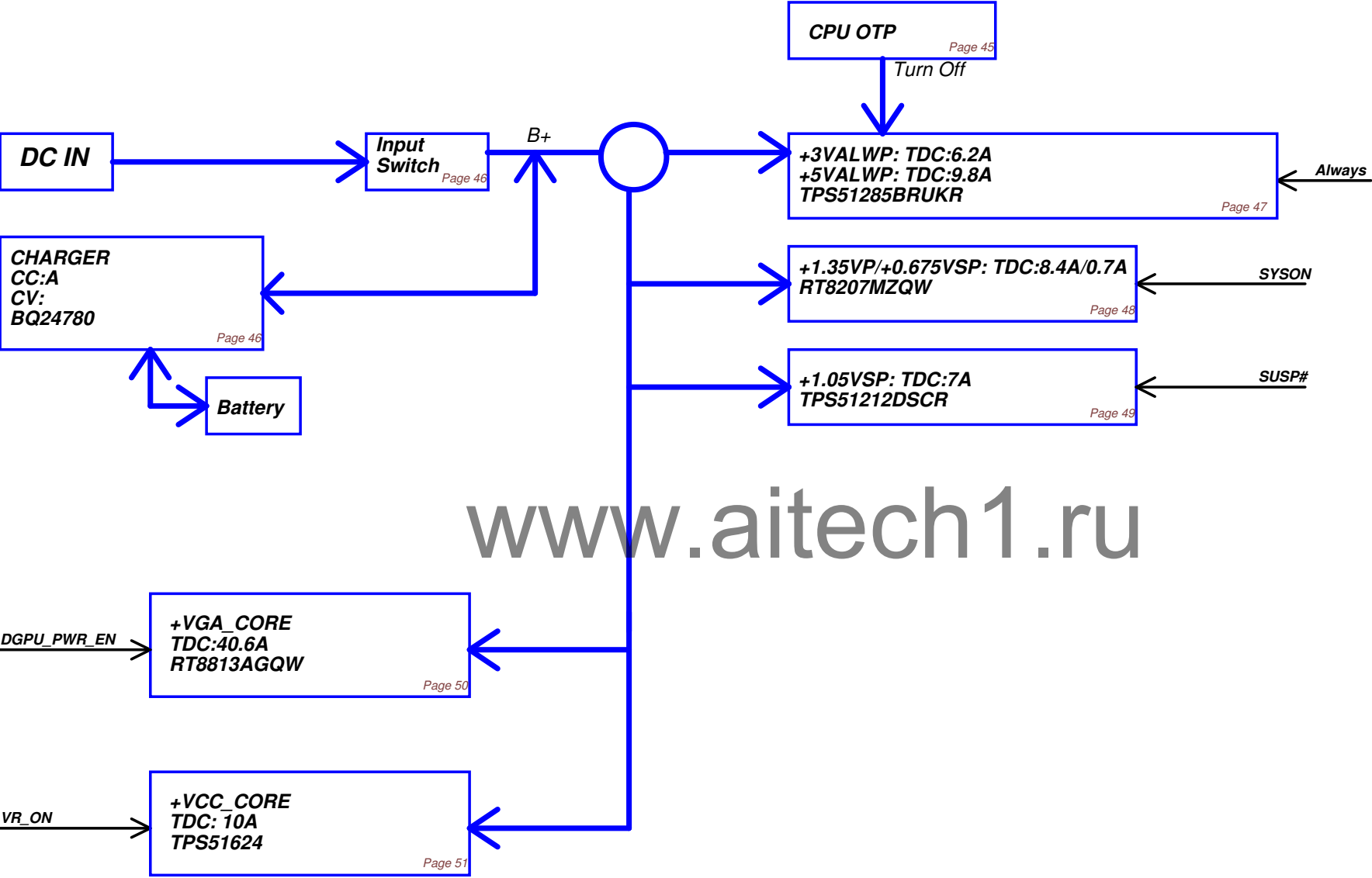
Local sense put on HW site

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				Date	Wednesday, March 26, 2014
				Sheet	65 of 69



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				Rev 0.1	
Date: Wednesday, March 26, 2014		Sheet 66 of 69			

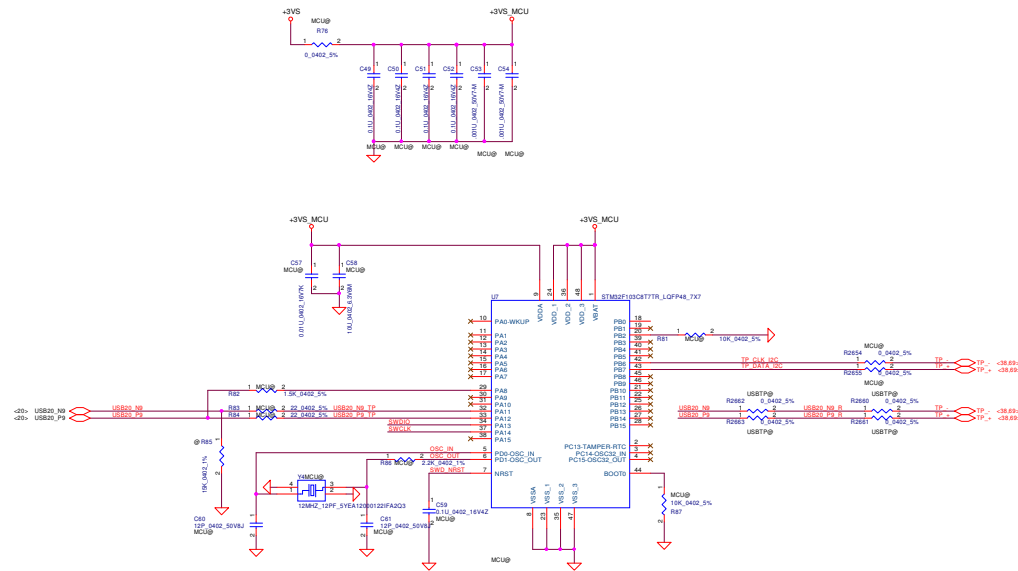
Power block



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Date: Wednesday, March 26, 2014				Sheet 68 of 69	



Reserved for debug

SWD_NST_R75 1 MCUUP 2 0.0402_5% T93
 SWDCLK_R99 1 MCUUP 2 0.0402_5% T94
 SWDIO_R109 1 MCUUP 2 0.0402_5% T101

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